Get acquainted with the semiconductor industry
Delve into the final step of chip manufacturing, the phase in which the chip is ‘packaged’ in its housing
Focus on the design and manufacturing of semiconductor packages and the associated assembly techniques
Education in the field of packaging

Without advanced packaged and integrated chips, we can’t live in smart houses, drive our autonomous cars or communicate through a 5G network.

Chip Integration Technology Center

Chip Integration Technology Center (CITC) is a non-profit innovation center that specializes in heterogeneous integration and advanced packaging technology. It is a place where companies, research and educational institutes work together on bridging the gap from academics to industry and create new and better solutions. Therefore we offer:

- Access to Innovation
- Access to Infrastructure
- Access to Education

Access to Innovation

One of CITC’s core activities is organizing and executing innovation programs in the field of packaging and integration technology for chips. Current program lines are:

- Thermal High-Performance Packaging
- RF Chip Packaging
- Digital Package Manufacturing
- Integrated Photonics Packaging

Access to Infrastructure

Providing access to lab infrastructure is one of CITC’s key capabilities. We maintain lab facilities that support the innovation programs but also support the education aspects that are relevant in the field of packaging, both students and company employees to get training in all the specific needs of the companies involved. This part-time course, with a duration of 5 months, enables both HAN students and company employees to get training in all the aspects that are relevant in the field of packaging, both theoretical and practical. The course includes a practical assignment that will be carried out on the premises of either a Semiconductor company or CITC.

CITC – HAN Semiconductor Packaging module

Together with the HAN University of Applied Sciences, CITC developed a Semiconductor Packaging module tailored to the specific needs of the companies involved. This part-time course, with a duration of 5 months, enables both HAN students and company employees to get training in all the aspects that are relevant in the field of packaging, both theoretical and practical. The course includes a practical assignment that will be carried out on the premises of either a Semiconductor company or CITC.

Access to Education

CITC collaborates with universities, applied universities and companies to support and provide packaging and chip integration technology related education. This includes internships, MSc/PhD programs and a specific CITC – HAN Semiconductor Packaging module.

We organize, in close cooperation with companies and educational institutes, targeted education and training for young talent. This is needed to secure the future of the Semiconductor Industry in Europe. By providing a connection between education and industry, CITC enables a flow of properly trained and skilled students that fit the needs of the industry. At the same time, ‘lifelong learning’ is supported by enabling existing employees to stay up to date on the latest developments in this industry.

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Class location - CITC building, Transistorweg 5T Nijmegen
Language - English
Study format - Part-time, 1 semester (about 6 Months)
Costs - If this is part of your bachelor program go to www.han.nl/kosten. If you do this as a stand-alone module, you pay €3,750,- excluding about €200,- in study material.
(Expected) start date - September 2020 or February 2021
Title/ Level - Bachelor/ University of Applied Sciences
Diploma - Certificate or part of your bachelor degree
Study load - ±20-24 hours per week (lectures + self-study)
Webbink for student participation - www.han.nl/deeltijd or www.kiesopmaat.nl/modules/han/-/141472/

Semiconductor Packaging module

Learn more about integrated chip technology and its applications with focus on the design and manufacturing of semiconductor packages and the associated assembly techniques.

Module

In the Semiconductor Packaging module you will get acquainted with the semiconductor industry and delve into the final step of chip manufacturing, the phase in which the chip is ‘packaged’ in its housing. Packaging is becoming more and more involved. Developments such as system-on-chip, embedded cameras, RF, sensors and Micro-ElectroMechanic Systems (MEMS) place high demands on the manufacturing process and the competencies of affected employees. Packages are becoming more complex and more customer-specific, while their serial size decreases. This module focuses on the design and manufacturing of semiconductor packages and the associated assembly techniques. The module was developed through collaboration between HAN University of Applied Sciences, CITC and its partners NXP, Nexperia, Ampelcon, TU Delft and TNO.

For whom

You are employed in semiconductor packaging or interested in it. Regular Bachelor students can follow this module as a minor.

Program

The module consists of 2 blocks of 9 weeks. In the first term you delve into the theory of semiconductor packaging and assembly. In the second term you design a semiconductor package together with a group of students and working professionals from the semiconductor industry. You also turn this design into a prototype to demonstrate its working principle and feasibility. The production and testing of the prototype takes place in the laboratory of CITC in Nijmegen or at one of the industrial partners. In parallel you study a number of elective subjects, depending on the project and your personal learning needs.

Assessment

The module assessment contains two parts:

1. An integral written test on the 4 knowledge areas, halfway through the module.
2. A demonstration at the end of the module. This is a group presentation in which you present the project and your individual contribution. In the presentation you:

- Explain your design choices;
- Demonstrate the prototype;
- Evaluate the tests;
- Substantiate the technical and commercial feasibility of implementation.

Subjects

The following subjects are covered in this module:

Term 1
- Semiconductor packaging introduction
- Advanced applications
- Basic simulation and testing
- Design Quality and Economics

Term 2
- You zoom-in on two topics that fit your personal learning needs and support the project:
  - Simulation (Multi constrains)
  - [Advanced] packaging materials
  - Quality control and reliability
  - Industrialization & Equipment
  - Testing
  - Data analysis

Admission

- For bachelor students: You have completed 2 main modules for Electrical and Electronic Engineering, Applied Physics, Mechanical Engineering, Automotive Engineering, or Industrial Engineering & Management.
- For working professionals: You have bachelor level work and thinking level and are employed in the semiconductor industry.
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Content

Theme 1 - Semiconductor and Packaging Introduction
1A Front-End
1A.1 Microelectronics introduction
1A.2 Semiconductor Physics overview
1A.3 Semiconductor materials (Si, SiC, GaN, ...)
1A.4 Basic process technology steps (litho, etch, doping, ...)
1A.5 Process Integration illustrated by a CMOS flow
1A.6 3D microstructuring for MEMS
1B Back-End
1B.1 Basic assembly and packaging steps (grinding, dicing, ...)
1B.2 Package families overview
1B.3 Die attach technologies
1B.4 Interconnect technologies
1B.5 Encapsulation technologies
1B.6 Application specific packaging -1 (IC, ...)
1B.7 Application specific packaging -2 (LED, ...)
1B.8 Application specific packaging -3 (RF, power, automotive, health)
1B.9 Application specific packaging -4 (MEMS & sensors)

Theme 2 - Advanced Applications
2A Application areas and associated requirements
2A.1 Packaging as an enabler for electronic mega trends
2A.2 Consumer (mobile, multimedia, IoT, ...)
2A.3 Industrial and B2B (passports, credit cards, machines, ...)
2A.4 Aerospace and Defence
2A.5 Health and Medical (ePills, microfluidics, sensors, lab-on-chip)
2A.6 Automotive (engine control, autonomous driving, V2X, ...)
2B Advanced Packaging techniques
2B.1 Water Level Packaging (WLP) principles
2B.2 WLP for ICs (WLCSP, FOWLP, POWLP, ...)
2B.3 WLP for MEMS (thermic sealing, openings, ...)
2B.4 3D integration technologies
2B.4a Embedded die
2B.4b Interposer technologies
2B.4c Through Package Vias (TPV)
2B.4d Through Silicon Vias (TSV)
2B.4e Micro bumps
2B.4f Die and water stacking
2B.5 Fundamentals of heat dissipation in 3D packages

Theme 3 - Simulation and Testing
3A Simulation
3A.1 Numerical methods in scientific computing
3A.2 Thermal simulations
3A.3 Mechanical simulations
3A.4 Design optimization
3B Testing
3B.1 Principles of testing
3B.2 Back-End test flow (wafer test, acceptance test, final test, ...)
3B.3 Tester functionality overview (architecture, probe cards, ...)
3B.4 Measurement accuracy (noise, calibration, sensing method, ...)
3B.5 Device parameters (breakdown, leakage, resistance, ...)
3B.6 Binning / Sorting
3B.7 Data Analysis & Water Maps
3B.8 Test Jobs (architecture, limits, ...)

Theme 4 - Quality, Reliability and Economics
4A Quality
4A.1 Basic quality control concepts
4A.2 Quality control in semiconductor packaging
4A.3 In- and off-line measurements and tests
4A.4 Quality program techniques such as CFD, DoE and SPC
4A.5 Quality control in the fabrication of packages
4A.6 Quality standards
4B Reliability
4B.1 Basic reliability definition, lifetime distribution and prediction methods
4B.2 Physical failure mechanisms in electronic components
4B.3 Package related failures
4B.4 Reliability screening and testing
4B.5 Failure analysis methods
4B.6 Design considerations and system reliability
4B.7 Thermal management in relation to package reliability
4B.8 Case studies of different package types (low/high power, ...)
4C Economics

More information
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