nano-silver / nano-copper paste vertical interconnects

Master's Thesis

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nano-silver / nano-copper paste vertical interconnects

THESIS

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in

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by

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Abstract

These a days the request for the reliability and the improved performance is becoming an important issue, particularly for the very small pitch of wafer level integration.

Nowadays, the demand for enhanced performance and reliability in micro and nano systems is growing, especially for fine pitch wafer level integration.Most TSVs are filled with copper

Potential for reliable environmental friendly low temperature interconnects relies in the exceptional properties of Metallic Nanoparticle Pastes (MNPs).Combined with lithographically based stencil-printing of copper paste, the study proposes an insight in optimization of the paste use for wafer level fine pitch vertical interconnection.Copper nanoparticle is investigated as interconnect material. Despite its high oxidation tendency, Copper is compatible with the current interconnect materials used in microelectronics, has good electrical properties and is cheap as compared to silver or gold. In commercial available copper MNPs, organic coating is added to protect oxidation and to enable sintering by a combined effect of coating evaporation and temperature increase.

Chapter 1

Introduction

One of the major applications of TSV is as an interposer,which is an electrical interface . Because of Mooreâs (scaling/integration) law, the silicon chip is getting bigger, the pin-out is getting higher, and the pitch is getting finer.

Most of the time through siclicon VIAs (TSVs) in wafers are filled with copper, At room temperature this is usually done with copper which has an expansion coefficient at 20 degrees Celsius of $\alpha = 17 \cdot 10^{-6} K^{-1}$[1]. All the material around the copper however, which is silicon has an expansion coefficient at 20 degrees Celsius of $\alpha = 2.56 \cdot 10^{-6} K^{-1}$[1]. From this can be seen that when this circuit gets heated up, a moment will come that the usual dielectric layer will not be able to hold the larger expansion coefficient and the more rapid increase of the thermal expansion of the copper will start causing cracks in the silicon. The solution for this could be to use powder made of certain materials instead of a copper bar through the vias, with other thermal expansion coefficients. When using this, it could solve the cracking of the silicon at higher temperatures. After manufacturing the wafer and making VIAs through silicon and filling these VIAs by ready nano-particle paste that we bought from the Locate Martine company, we should bake the wafer to making the particles being defused to each other

In this thesis are two different experiment was done, At a first step VTSs (via through silicon) are made on the double side polished wafer and was examined the filling process with nano paste metals , nano-silver and nano-copper paste. one issue here was to find an efficient method for the filling of VIAs. Initially was used a device

1.1 MOTIVATION

1.2 OBJECTIVES

1.3 ORGANIZATION OF THE THESIS

Chapter 2

THROUGH SILICON VIA TEST STRUCTURE DESIGN

2.1 INTERCONNECTIONS

IC integration previously sued to be done by 2D (two dimensional) techniques. For the recent expending and requirement of electronic clients market, The 2D integration techniques is inappropriate due to his sever problems and constraints in computing,wire communication and wireless systems. The vertical integration for having more efficiency and more condensed packages with the better integration flexibility of different technologies. Recently lots of researches and studies for finding new methods which can result into integration and miniaturization need for portable and advanced electronic devices.
There are different types of 3D packaging depending on the stacking techniques. Some of them are:

- 3d integration on chip in which practical layers in a chip are constructed, layer to layer
- die to die
- package to package
- 3D ICs with the integration made by TSV technique.

3D technology, like any other new techniques has his own challenges to beat in early stage before being accepted by the industry. And the challengers are low cost structures, simulation tools, reliable design and VIA filling processes. Today the tendency of the industry is directed from 2D into 3D due to it's better performance, power consumption, functionality and form factor [1].

2.1.1 Silicon Through VIAs (TSV)

Now a days interconnects technology as a result of it's better performance than classical interconnect technologies and a vast applicable area, extending memory and imaging products to to high speed logic and processing applications. The TSVs have many advantages rather than other classical 3D packaging techniques, such as making possible the construction of higher aspect ratio and higher density connections, which result into integration of multi-chip systems inside the silicon with the more efficient packing density rather than classical 3D packaging techniques.
The TSVs can removed the requirement of wire bonding. They also have the capability of implement of short connections, similarly short as the thickness of the chip, decreasing a lot the distance of the information flow on a chip (approximately to 1000x). Therefore they are not depending only on the area of the dies, as wire bonding, additional pathways and channels are. They are also be accessed more up to 100x than 2D chips. The restraints of of classical 3D packaging techniques can be resolved with 3D stacking TVS electrodes.
There are two variant ways for vertical VIAs based on the application type, which are adopted for 3D chip stacking like via first and via last. In the first via method, the VIAs are filled from the front side of the wafer similarly as the copper damascene applications. The first via method is shown in the following figure.

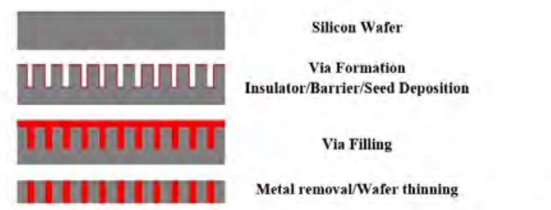


Figure 2.1: Blind-via filling before wafer thinning[1]

By exposing the TSVs, the wafer become thinner after the filling the VIAs. In the last VIA stacking method, the VIAs are filled after the wafers are thinned. The VIA last method is shown below. In the industry now a day the first method became more

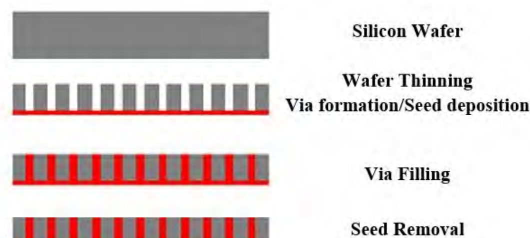


Figure 2.2: Through-via filling after wafer thinning[1]

popular due to the fact that it's difficult to handling and plating the thin wafers. The principle steps of the first method are as follow:

- Ethcing VIAs thought silicon using deep reactive ion etching (DIRE) laser method.

- Deposition of an insulator such as SiN or $Sino_2$by means of PECVD (Plasma enhanced chemical vapor deposition.
- Barrier deposition with *TiN* or *TaN* by means of PVD or MOCVD (metal organic metal organic chemical vapor deposition).
- CU (copper) seed layer deposition for having conductive layer, by means of CVD (chemical vapor deposition and PVD (Plasma vapor deposition) techniques. PVD process needs a lower temperature during the process and provide enough adhesion but undesirably has no uniformity. In CVD process needs the average temperature and efficient uniformity, also week adhesion.
- Filling the VIAs
- Thinning the wafer
- wafer or chip initially aligning and further bonding and dicing.

The copper deposition is the most favorable method between metal depositions , because it results into the complex and stable achievement. Moreover electrode deposition process needs cheaper equipment and the process are more simple to control and maintain, rather than vacuum based processes. For the big features poly silicon material is more appropriate, even though the copper has a better thermal and electrical properties. Poly silicon material has a comparable thermal expansion (CTE) with silicon. Copper has thermal expansion five to six times more than silicon and this stress in larger VIAs which can leads into the breakage of the wafer.For this reason Polymer coating is more appropriate method for filling the VIAs. Choice of the most suitable material and it's deposition, depends on wafer design with the changes in feature size, aspect ratios and cost, reliability and characteristics of the process.
The preferable industry method for VIA filling is the copper electrode deposition in TVS performance, because of his successful applications in PWB and copper damascene in the past [1].

2.2 MASK DESIGN

For bringing circuit patterns into silicon wafers and built the most critical stage in the flow chart of IC fabrication, which is similar to photographic printing ,The optical micro lithography is used. Initially the pattern is built on reticle or mask and then will be copied into the wafer as is shown in the following figure.

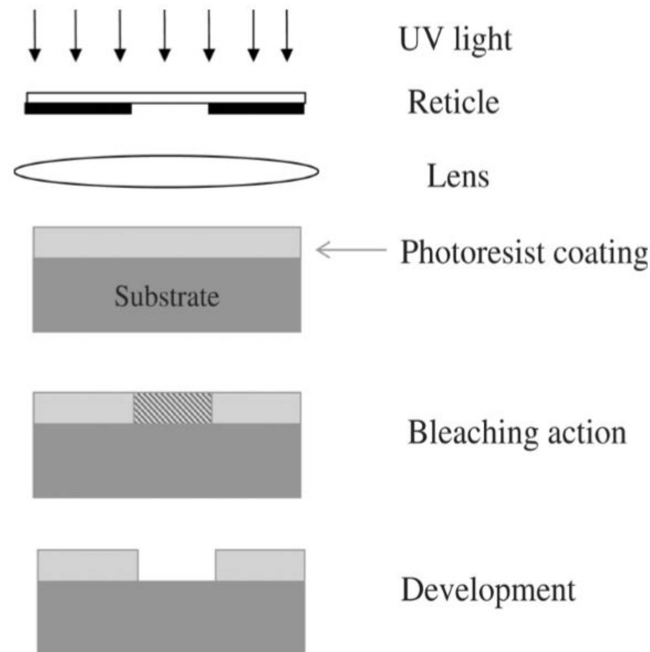


Figure 2.3: Steps involved in optical micro lithography[2]

By means one UV light source, UV light would be shine through the mask which built a copy of the pattern through the lens into the photoresist which is coated on the top the silicon wafer. the reduction factor sue for this system is 4X. The photoresist is the chemical which is sensitive to the UV light therefore the areas which are exposed by light would be developed away and creating a copy of mask on the wafer. A photomask is opaque reticle with transparencies and holes which the UV light would be shined through it to built a copy of the pattern. A series of photomasks which are most common are used and any individual one of to built a pattern layer in micro fabrication and this mask will place inside the photo lithography scanner or stepper and is selected for the required exposure.
In double patterning technologies,the layer pattern is related to a subdivision.
Before going to lithography the first step would be,designing the pattern for this opaque mask, which usually is done by a software named L-edit. And then the pattern will be transfer into a piece of glass and this glass is used to transfer the pattern through by exposure of the UV light.
The physical properties of each individual built at nano fabrication are:

- 5x5 light glass

- 0.09 thick chrome coated.

In nano fabrication, the L-edit which is the standard CAD tool is used.
The L-edit is able to make designs suitable for Nano fabrication and is not just the CAD program.
It's possible to use any other program which has the ability of making GDSII format output film. AS the L-edit is the most common used software for this purpose has the advantage to having a trouble shooting by the staff in Laboratory, while using other program would not providing this advantage.
For this reason is fully adjusted to use L-edit software, except that having the experience and be well skilled for other CAD programs.
In this project the L-edit software was used. And the copy of the multilayer photo mask is shown as follow. As seen different structures are available for the measurement on this design such as:

- Sheet resistance structure,
- Kelvin structure
- Daisy chain
- Electrical coils
- Capacitors
- Via text structure
- RF measurement structures

Each structure would presented and measured in the result and discussion chapter. The mask used in this project has the following characterizations:
Mask name:
$SUEX01_V1Box$: 413
Type: Multi image $3x3$
Exposure job(s): $Die6mm_9imgs$

Design layout

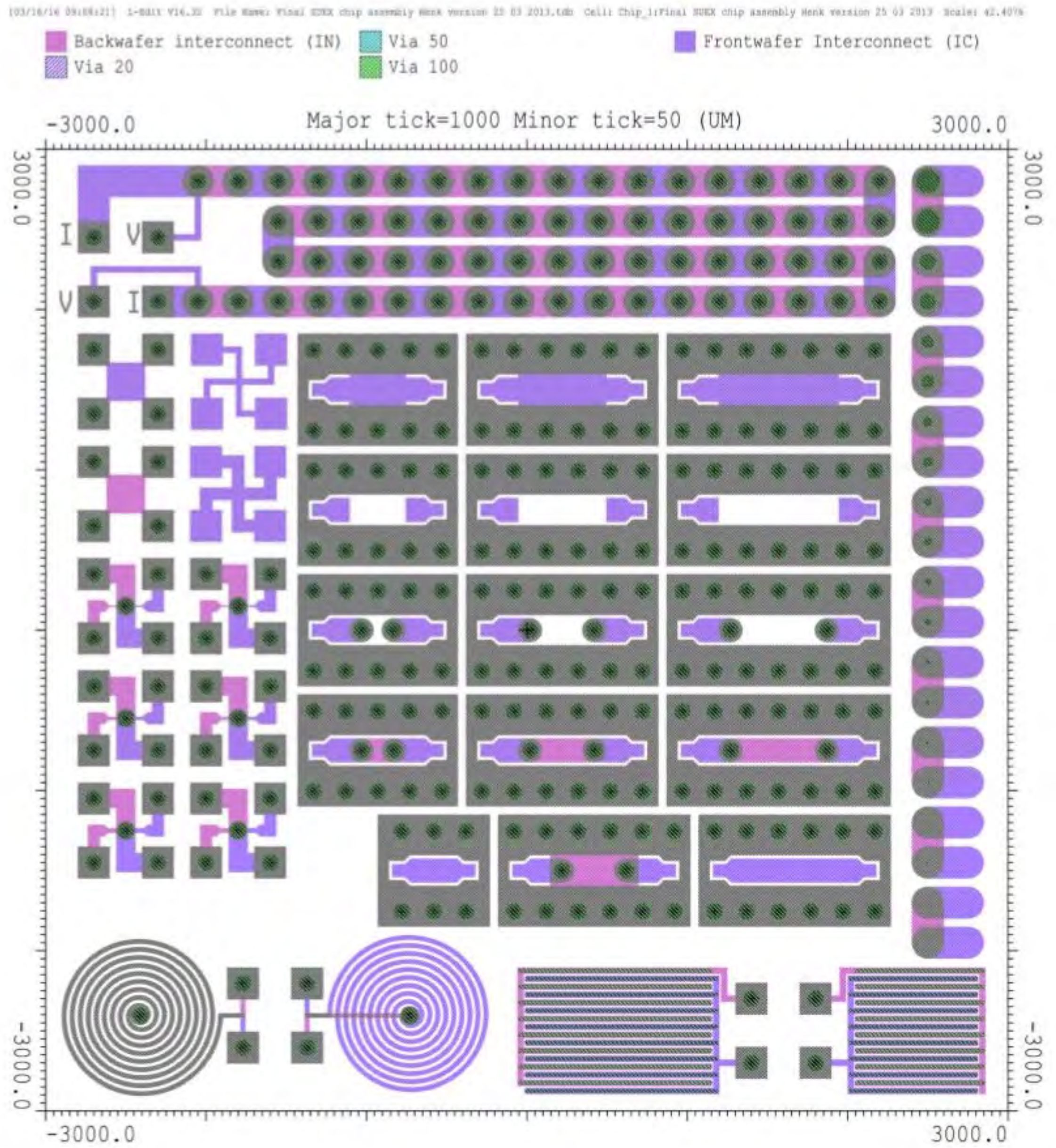


Figure 2.4: SUEX01_V1 multiimage 3x3 mask[]

2.3 Bulk resistivity

The bulk resistivity (ρ), which depends on drifting of carriers in materials like semiconductors and metals, is an intrinsic electrical property of the material. To measure a bulk resistivity , can be used a geometrical dimensions shown in the following figure (2.3), which is seen the cross sectional area in which passes current ($A = wt$) and the length between two contacts (L).

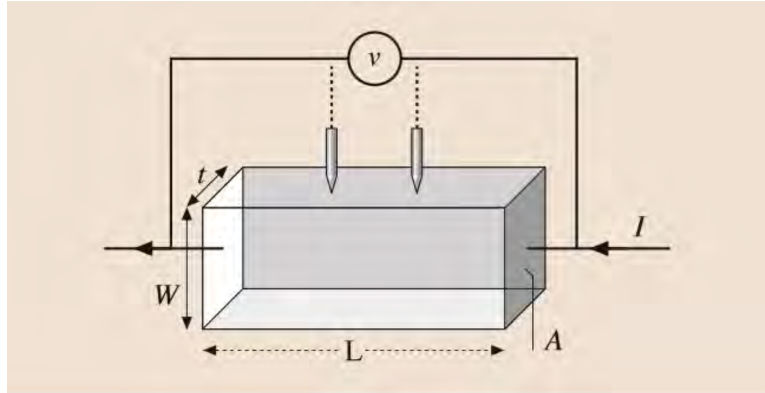


Figure 2.5: Bulk resistance and its geometrical dimensions[3]

The general equation for the resistivity is:
$\rho = RA/L$ [Ωm or ωcm]
In microelectronics for the thin layer of semiconductor sheet Resistance is used (R_s)
The sheet resistance is a particular type of bulk resistance in which resistance is divided by sample thickness (t) and the width is equal to length, there is square shape (W=L).
Area is A=wt, therefore sheet reistance is $\rho_s = R_\square$.
The unit of measurement for the sheet resistance is $\Omega/\square$ or Ω/square. The sheet resistance ($R_\square$) is more appropriate because it gives the possibility of the fast design of the geometry for any particular value of the resistance by means of thin implanted or diffused semiconductor areas or poly crystalline layers to circuit designers. The conductivity σ, which is the inverse of the resistivity with unit of the measurement of $\Omega^{-1}cm^{-1}$ or S/cm, is useful to categorize material into metals, semiconductors or insulators by using the it's change due to the variation of temperature.
The resistivity is not the essential parameter for material and it's possible respectively having the same resistivity for different materials and also different values of the reisistivity for one material, which depends on the process. Based from the state solid theory in a homogeneous semiconductor materials the resistivity can be defined as the proportion relation between applied electrical field (E) and the drift current density (J) as follow:

$$J = (1/\rho) \tag{2.1}$$

$$\rho = \frac{1}{q(n\mu + \rho\mu_p)} \tag{2.2}$$

In which q is electronic charge, n is electron concentration, P is holes concentration, μn is electron mobilities drift and μp hole mobilities drift.
From this equation is seen that resistivity is depends on important intrinsic parameters of semiconductor such as amount of free carriers and the potential move of the in the lattice where also the electrical field is applied.
The free carrier density for the for $n-type$ (donor ND) or $p-type$(acceptor NA) doped semiconductors, is defined by NA and ND (ionized impurities). The intrinsic carrier concentrations can be reduced as follow:

$$\rho \approx \frac{1}{qp\mu_n}, \quad \text{for n-type} \tag{2.3}$$

$$\rho \approx \frac{1}{qp\mu_p}, \quad \text{for p-type} \tag{2.4}$$

These equations are concerned just for the single type of semiconductor. In this project there also some structure, as shown in following figure are added to the mask for the measurement of the sheet resistance.

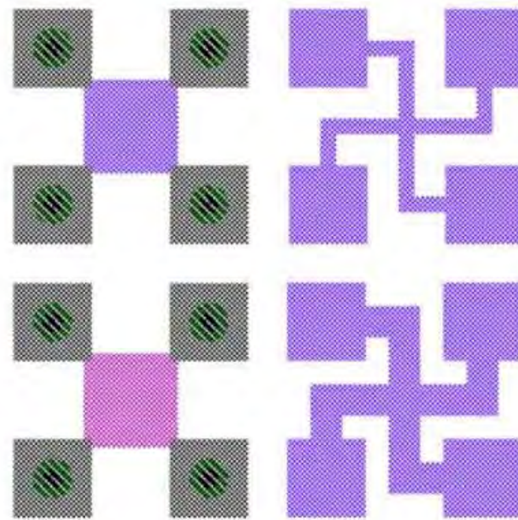


Figure 2.6: Structures for the measurement of the sheet resistance

Figure 2.7: Back side wafer interconnect (IN)

Figure 2.8: front side wafer interconnect (IC)

The whole procedure of measurement and the result is discussed in the results chapter [3].

2.3.1 MEASUREMENT TECHNIQUES

One of the common method to measure the resistivity of the bulk is to flow the dc current along the bar sample of silicon and then measure the voltage drop and by using the equation for the resistivity is possible to find a value for the resistivity of the sample. But inappropriately the measure Resistance (R_m) include also the contact Resistance which can be dominant in the small size of the sample. And in the case that the probes are used instead of metal semiconductor contact, is added also the spreading Resistance (R_{SP}) of the probes.

$$R_m = R + 2R_{sp} + 2R_c \tag{2.5}$$

we assume the sample is semi infinite. For the cylindrical contact with radius r,

$$R_{sp} = \frac{\rho}{4r} \tag{2.6}$$

For a hemispherical contact,

$$R_{sp} = \frac{\rho}{2\pi r} \tag{2.7}$$

some techniques are shown further to reduce the effect of spreading resistance but still the accuracy of the measurement is not guaranteed.

The measurement techniques for the bulk resistivity are:

- The four-point-probe technique.
- The van der Pauw technique.

And the measurement is presented for the contact resistivity is:

- Transmission line model test structures
- Kelvin contact Resistance (KRC) [3].

THE FOUR-POINT-PROBE TECHNIQUE

One of the simplest method of the measurement is two probe technique which is shown on the figure 2.1, but this method has some disadvantages such as lateral contact geometry, Probe spacing, and minority carrier injection near the later contacts. One of the method to reduce the main disadvantage which is the need for lateral contacts called the four point probe technique. In this technique Two probes are used for the current injection and the two other remaining probes are used for measuring the voltage drop.This configuration is shown in the figure 2.2. Where the t is thickness and a is the distance from edge of the sample.the voltage prob on prob 1 and 4 which is induced by applying a current to probe one to probe four is:

$$V_2 = \frac{\rho I}{2\pi}.(\frac{1}{S_1} - \frac{1}{S_2 + S_3}) \tag{2.8}$$

And the voltage drop at probe 3 is:

$$V_3 = \frac{\rho I}{2\pi}.(\frac{1}{S_1 + S_2} - \frac{1}{S_3}) \tag{2.9}$$

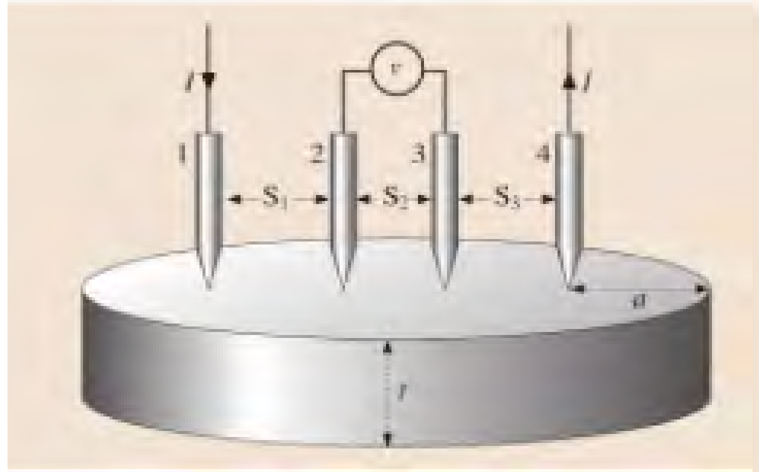


Figure 2.9: Linear four probe configuration [3]

For defining the resistivity we have to measure the voltage drop between probe 2 and 3 ($V = V_2 - V_3$), and the Current I through probes 1 and 4.The resistivity is as follow:

$$\rho = \frac{2\pi V/I}{(\frac{1}{S_1} + \frac{1}{S_2} - \frac{1}{S_2+S_3} - \frac{1}{S_1+S_2})} \tag{2.10}$$

when the prob spacing are equal ($S_1 = S_2 = S_3 = S$) the equation is as follow:

$$\rho = 2\pi S.\frac{V}{I} \tag{2.11}$$

Two previous equations are valid only when the thickness and surface are very large.In the case of the finite thickness and surface a correction factor (f) should be added to the equation to consider the effect of finite thickness and surface of the sample and it's boundary effects. For homogeneous layers, f should taking into account the intrinsic properties of the material either is an conductor or insulator.
The equation for the resistivity becomes as follow:

$$\rho = 2\pi S.\frac{V}{I}.f \tag{2.12}$$

For the case of thin wafers or thin deposited layers on the substrate and for the particular case in which the distance between probes (s) is bigger than 2 times of the thickness $t < s/2$ this present another case , because usually the distance between probes is in the order of millimeters so the correction factor and reisstivity would be:

$$f = \frac{(t/s)}{2ln2}, \quad \text{so that,} \quad \rho = 4.532t\frac{V}{I} \tag{2.13}$$

If the ratio of the wafer diameter to the distance between probes is less than 40, then the non infinite sample outer surface should be corrected, alternatively the correction factor less than unity should be used. In the case that the head of the prob is near to any boundary, (2.13) is not valid anymore and then another correction factor should be used. In this case the correction factor is close to unity till the ratio of a/s is more than

2. where the a is is the distance from the edge of the substrate which is illustrated in the figure 2.7. If another configurations of four point prob is used like the case in which the current passes between probes 1 and 3, other correction factor should be used.
For having a better accuracy (better than 1%) in the measurement of the resistivity of various type of semiconductor wafers or deposited thin semiconductor layers, should considered carefully the right correction factor and other parameters of the material like surface oxidation or hardness and the usage of appropriate equipment and calculations method [3].
In this project the current is passes through probe 2to probe 4 and the voltage is measured between probes 1 and 3 as show in follow.

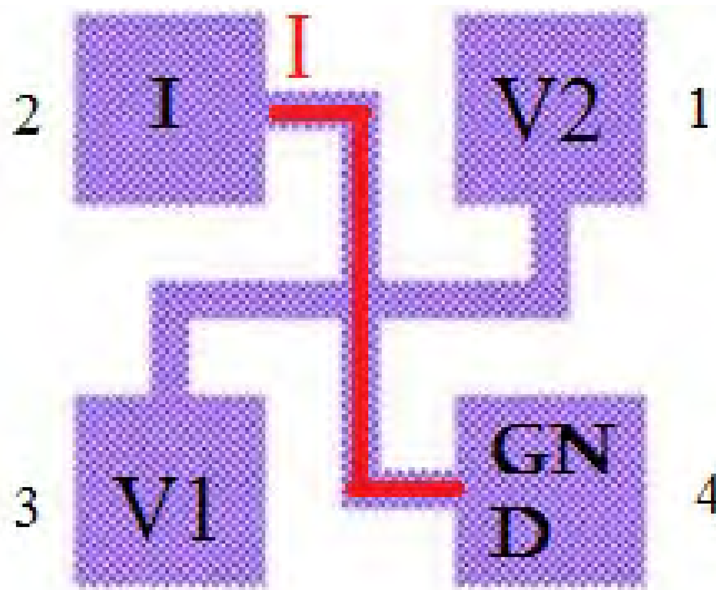


Figure 2.10: Sheet resistance text structure

Van der Pauw Technique

The concept of this technique is based on the separating the current injection and the voltage measurement and called Van der Pauw. This technique for the measurement of the reisitivity four probes on a sample with the arbitrary shaped will placed which is shown in the following figure.

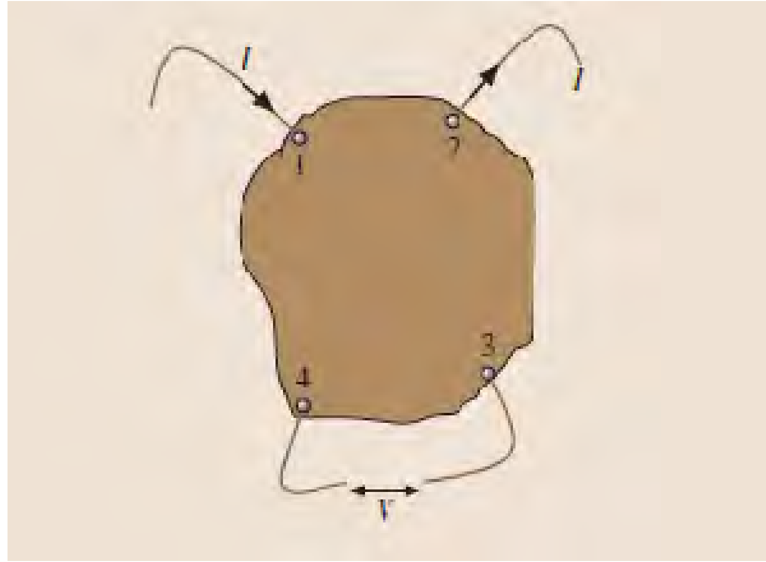


Figure 2.11: van der Pauw method for an arbitrarily shaped sample[3]

The resistivity for the homogeneous sample with the thickness of t is:

$$\rho = \frac{\pi t}{Ln2} \frac{R_A + R_B}{2} f \tag{2.14}$$

The Resistance R_A and R_B are measured by forcing the current into two adjacent contacts and measure the voltage of two other contacts.
With the reistances of:

$$R_A = \frac{V-3-V_4}{I_{1,2}} \qquad R_A = \frac{V_4 - V_1}{I_{2,3}} \tag{2.15}$$

Where the f is the correction factor which depends on the following ratio:

$$R_f = \frac{R_A}{R_B} \tag{2.16}$$

Which is achieved from:

$$\frac{(R_F - 1)}{(R_f + 1)} = \frac{f}{Ln2}.arccosh(\frac{EXP(Ln2/f)}{2}) \tag{2.17}$$

In the following figure some of example of symmetrical geometries therefore $R - A = R_B, R_F, f = 1$ and the resistivity is:

$$\rho = \frac{\pi t}{Ln2} R_A = 4.532 t R_A \tag{2.18}$$

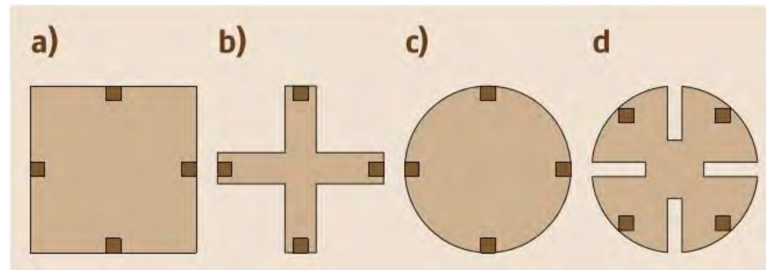


Figure 2.12: Symmetrical van der Pauw structures: (a) square, (b) Greek cross, (c) circle and (d) cloverleaf [3]

To reduce errors due to the contact area which is not zero and not zero thickness of the sample, The space between contacts should be bigger than the two of the thickness of the contact and it's diameter. The clover leaf shape is most advised configuration because it is avoiding contact misalignment but disadvantage of this shape is the complexity of it's patterning.
One the most important benefits of the van der Pauw rather than the four point probe method is the less area used for the test structure. And this method is the most common used method in the integrated circuit technology.
The Greek cross shape due to his simple structure, is also largely used. The undesired current crowding caused due to narrow arms, can be reduced by using another Greek cross layout [3].

2.4 CONTACT RESISTIVITY

By scaling dimensions of device and interconnections, the contact resistance will increase.
A transistor similarly to an integrated circuits can depends on enlarging of the power consumption and the RC time constants. This is an important issue in the semiconductor industry [3].

2.4.1 Contact Resistance Elements

The resistance of the contact pad such as a probe or a metalization which is connected to the active region, called contact resistance (R_S). In the following figure is shown that this not including all the access resistance between two regions, part a is referred to a horizontal and part b is referred to a vertical contact. The contact resistance is

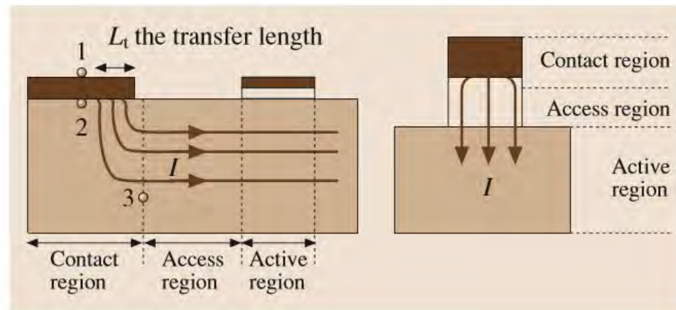


Figure 2.13: Blind-via filling before wafer thinning[3]

consisting of the metal resistance (R_m), the interface metal semiconductor resistance (R_i) and the resistance related to the semiconductor which placed under the contact in the contact region (R_{sc}). Therefore the contact resistance which is shown in following picture is:

$$R_C = R_m + R_i + R_{sc}. \tag{2.19}$$

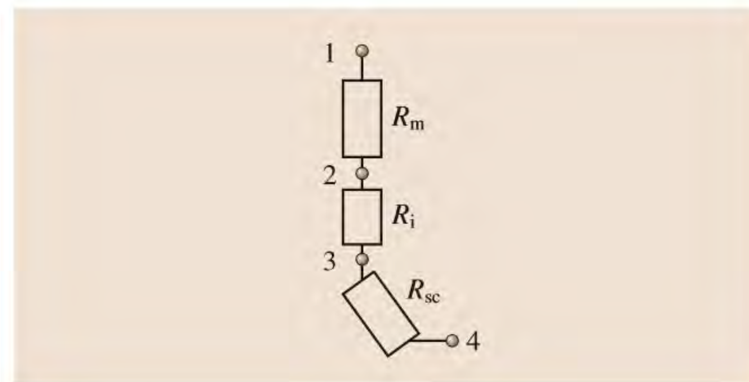


Figure 2.14: Different components of the contact resistance [3]

The R_{sc} resistance is not easily calculable due to difficulty to determine the boundary between the contact and access region and this because of inter diffusion of semiconductor and metal atoms and the non homogeneous current passing through this area due to the current spreading and the vertical or lateral current crowding in the contact area. Different parameters such as the annealing temperature of the procedure, doping density and geometrical shape like being vertical or lateral, can define the significance of each individual component of the contact resistance. The most useful factor by comparing of variant areas and methods,the contact resistivity (ρ_C) and that is particular type of contact resistance in unit of measurement of Ωcm^2 which can be expressed as follow:

$$\rho_c = R_c A_{ceff} \tag{2.20}$$

A_{ceff} is the effective is the significant contact area which the current injection area. The right side figure in the figure 2.13 is the good geometrical approximation for the definition of an effective contact area in the vertical configuration. In the lateral contact case, determining the A_{ceff} is more challenging where LT is a transfer length which introduce the length that the current flow passes from the contact into the right underneath of the semiconductor.
LT is the length in which the voltage value is e^{-1} and is expressed as follow:

$$L_T = \sqrt{\frac{\rho_c}{\rho_{sc}}} \tag{2.21}$$

The ρ_c is the sheet resistance of the semiconductor under the contact. It is really challenging to model precisely the contact resistivity due to having different components. The interface resistivity ρ_i can be defined by schotty theory of metal semiconductor contacts as follow:

$$\rho_i = \frac{\partial V}{\partial J} \mid v = 0 \tag{2.22}$$

As the metal semiconductor junction can be assumed as a p-n junction, therefore the J-V characteristic of the metal semiconductor in low doped case is:

$$J = A * T^2 exp(-\frac{q\phi_B}{KT})[exp(\frac{qV}{KT}) - 1] \tag{2.23}$$

A* is Richardson's constant, T the absolute temperature and ϕ_B is the barrier height in the interface of the semiconductor metal. ϕ_B is the difference level between vacuum and Fermi level of the metal and the semiconductor as follow:

$$\phi_B = \rho_M - \chi \tag{2.24}$$

ϕ_M is the metal work function and χ is the electron affinity of the semiconductor.
In the following figure is dimostrated n-type low doped semiconductor metal contact. There is a rectifying contact due to fact that the transport current is more significant than the thermionic emission current.
The interface resistivity when depends on the thermionic emission is:

$$\rho_{i,TE} = \frac{k}{qA * T} exp(\frac{q\phi_B}{KT}) \tag{2.25}$$

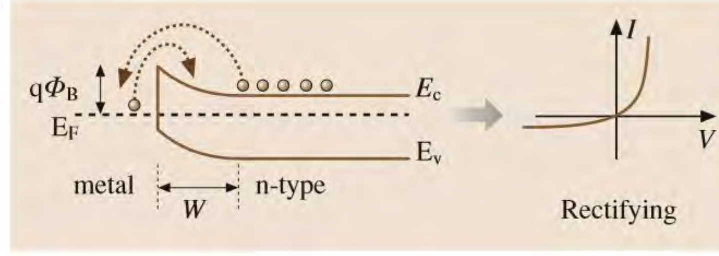


Figure 2.15: Energy-band diagram of an n-type semiconductor-metal contact and related rectifying contact. W is the width of the depletion layer [3]

The barrier height ϕ_B is positive and not much depending on the semiconductor metal material because of the existence of the surface states.

$\phi_B \approx 2E_g/3$ for n type
$\phi_B \approx E_g/3$ for p type

Excluding the case of narrow band gap semiconductors, large values for interface resistivity ($\rho_{i,TE}$) is achievable. By processing the metal on a heavily doped semiconductor layer, ohmic contacts with low contact resistivity can be constructed.
In this situation by enlarging the the depletion width ($W \approx N_D^{-1/2}$),the probility of the carrier tunneling through the barrier getting larger. Therefore there is significant tunneling is shown in the following figure.

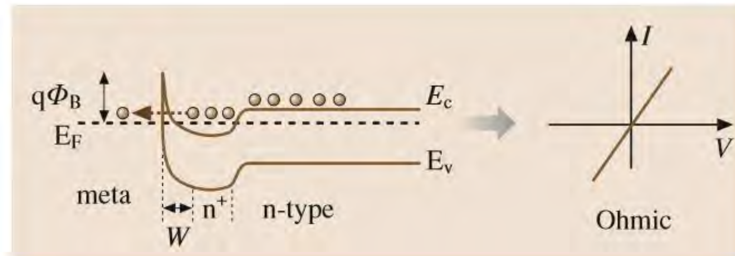


Figure 2.16: Energy band diagram of an n^+-n semiconductor metal structure and related ohmic contact [3]

The electron tunneling current is:

$$J_{tun} \approx exp(\frac{q\phi_B}{E_{00}}) \tag{2.26}$$

And

$$E_{00} = \frac{q\hbar}{2}\sqrt{\frac{N_D}{\varepsilon_s m_n^*}} \tag{2.27}$$

ε_s is the permittivity semiconductor and m_n^* is the effective mass of the electron.

And finally the interface resistivity $\rho_{i,T}$ is:

$$\rho_{i,T} \alpha \frac{2\sqrt{\varepsilon_s m_n^*}}{\hbar} \cdot \frac{\phi_B}{\sqrt{N_D}} \tag{2.28}$$

From comparing two presented equations of ρ_i and $\rho_{i,T}$ can be observed that the interface resistivity decreased a lot by a highly doped layer.
For $N_D \geq 10^{19} cm^{-3}$ the interface resistivity depends on tunneling process, while for $N_D \leq 10^{19} cm^{-3}$ the interface resistivity depends on the thermionic emission current.
The deposition of the heavily doped layer before metallization to built a tunneling contact in semiconductors such as Si, SiGe, GaAs and InP.
The contact layer is usually constructed from the same semiconductor material or the same material of the substrate, for compound semiconductor constructing procedure. The silicidation methods are more usual to built the contact layer with thin silicide layers like $TiSi_2$ or $CoSi2$, for silicon , SiGe alloys or polysilicon [3].

2.4.2 Measurements Techniques

Transmission Line Model Test Structures

The test structure which include the metal grid pattern deposition of not equal distance between contacts (L_i), called The transmission line model test structure (TML). The result is the planar resistor structure. Any individual resistor in this structure varies with it's distance between two adjacent contacts (L_i) and is defined as follow:

$$R_i = \frac{\rho_s L_i}{W} + 2R_c \tag{2.29}$$

In sequence the sheet layer resistivity (ρ_S) and the contact resistance (R_c) can be calculated from the slope of the plot of measured resistance vs. distance between contacts (L_i) as is shown in the following figure.

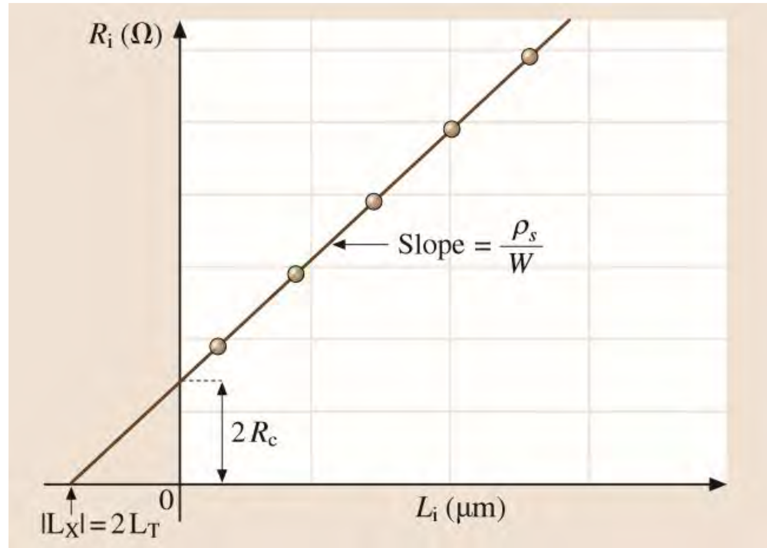


Figure 2.17: Determination of the sheet resistivity and characterization of the contact using a TLM test structure [3]

At $L_i = 0$ then slope is : $\frac{\rho_s}{W}$;
R_i (intercept) = $2R_c$;
and $|L_i(intercept)| = 2L_T$
For the calculation of a contact, the contact resistivity ρ_S and the spesific contact resistance $R_c A_{ceff}$ are essential factors and are:

$$\rho_C = R_c A_{ceff} = R_c W L_T \tag{2.30}$$

Previously was demonstrated that for a planar resistor the contact effective area depends on transfer length which is:

$$L_T = \sqrt{\frac{\rho_c}{\rho_{sc}}} \tag{2.31}$$

Where ρ_{sc} is the sheet resistance below the contact and ρ_c is the sheet resistance between the contacts.

And R_i would be as follow:

$$R_i = \frac{\rho_s}{W} L_i + \frac{\rho_s}{W} 2L_T \tag{2.32}$$

At the end by $R_i = 0$ it's possible to define the value of L_T.
This method is useful for achieving two important electrical properties such as the contact resistance (R_c) and the contact layer of the semiconductor (ρ_s). This is valid under the assumption of the equivalence of the sheet resistance below the contact with the sheet resistance between contacts [3].

Kelvin Test Structure

The cross Kelvin resistor (CKR) or the Kelvin test structure is presented in the figure below. To define the contact resistance (R_C), a current is forced from contact pad 1 to

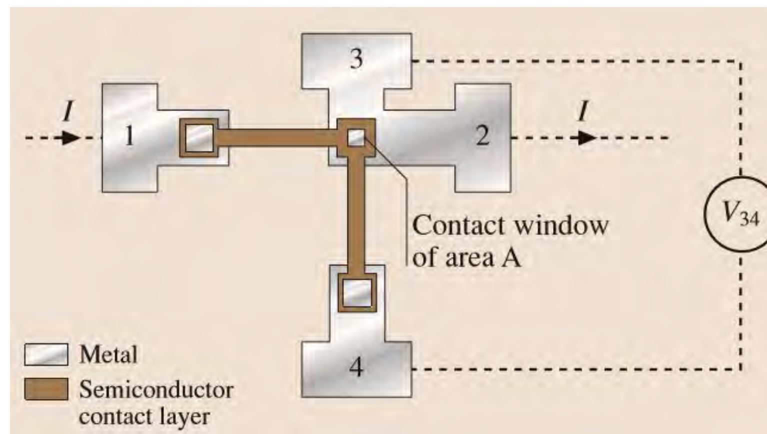


Figure 2.18: Cross Kelvin resistor test structure [3]

contact pad 2 and the voltage drop between pad 3 and 4 would be measure. the contact resistance is:

$$R_C = \frac{V_{34}}{I} \tag{2.33}$$

By knowing the contact resistance (R_C) and the area (A) is the contact resistivity is obtainable as follow:

$$\rho_C = R_c A \tag{2.34}$$

In the case that the parasitic effects are existing, this equation is not valid anymore.
The current crowding is also an essential problem around the contact.
The two dimensional current crowding effect should be considered to achieve a precise value in the measurement of the contact resistivity by Kelvin test structures. And this obtainable by means of using numerical simulations.
For construction of ohmic contacts with the very small values of the contact resistivities, more complicated method with variant materials and mostly multiple interfaces are needed. There is a big difference between the calculated and the measured contact resistance.
To improve and make this value more precise, the three dimensional models with considering the variant interfacial and vertical parasitic effects are used [3].

In this project there are different text structures, For example the kelvin structure which is shown in the following figure.
In this structure there two contact resistance on the top and bottom point of the connection between the sputtered copper surface and the via filled by nano copper particle pastes. The total Resistance for each structure is:

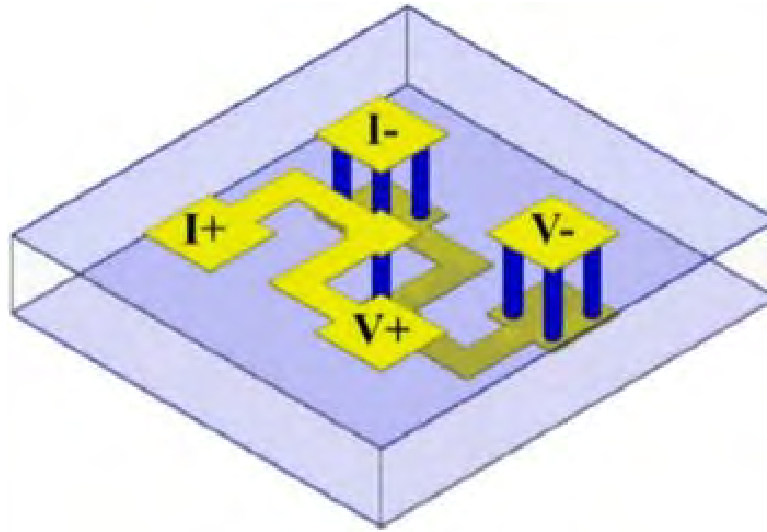


Figure 2.19: General kelvin test structure [4]

$R_{total} = R_{c1} + R_{via} + R_{c2}$ There is no accurate calculation for finding the contact resistance value. The interest here is finding the resistance of the via (R_{via}) and in sequence the resistivity of the nano copper paste which were used for filling the VIAs.

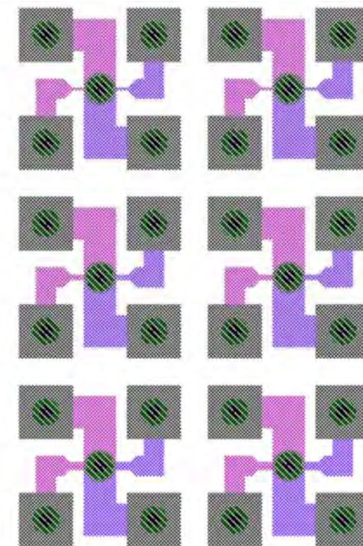


Figure 2.20: Kelvin test structure used in this project.

2.5 Chapter conclusion

In this chapter the interconnections and included resistances in device and different method of measurement and some test structures are discussed.

Chapter 3

EXPERIMENT AND FABRICATION

3.1 SILICON WAFER CHARACTERISTICS

A silicon wafer or substrate is a thin circle of the semiconductor material (silicon Crystal) as shown in the following figure, which is used in micro fabrication for manufacturing the integrated electronic circuits.
This wafer would be the substrate for the device and will be processed further by different procedures like ion implantation, doping, etching, thin film depositions of different materials, lithography patterning and etc. And at the end these devices would be diced into smaller dies and packaged [5].

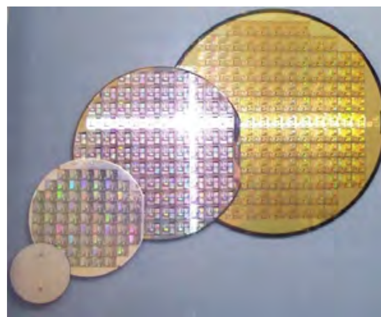


Figure 3.1: Silicon wafers [5]

The characterization of the wafer which were used in this project is as follow:

- Double Side Polished wafers (Double side polished low resistivity (Lres) wafers
- Thickness: 310um
- Quantity: 9

3.2 LITHOGRAPHY

Lithography is originates from a Greek word of Lithos and write as grÃ¡phein which was invented by Aloys Senefelder in 1796. This person discovered the Bavarian limes stone which by means of ink and chemicals could have transfer any figure to the paper. Transferring the pattern to a photosensitive chemical (photoresist) and then exposure it by the light source thought the optical mask, is most common method for the lithography.
An optical mask with opaque patterns of the chrome or the iron oxide for transferring the patterns on the wafer is used. In the following figure a simple schematic of the lithography is shown.

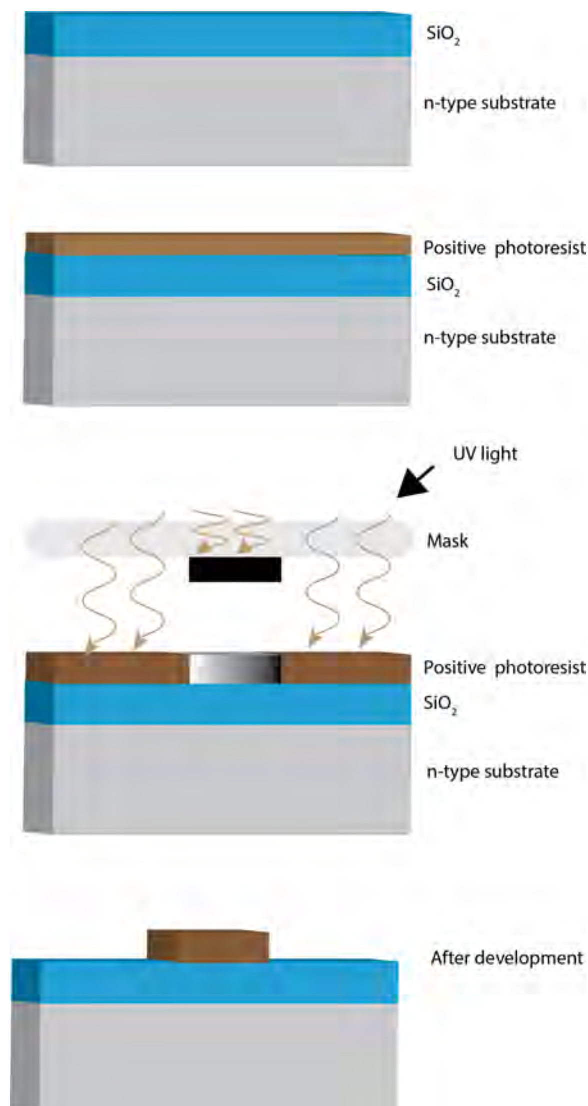


Figure 3.2: Lithography

This pattern can be also transferred to the other layers or substrate by means of etching or additive layer deposition. In this project the following steps for the lithography were

done:

- coating zerolayer
- Alignment and Exposure
- Development

3.2.1 PHOTORESIST COATING FOR ZERO LAYER

In this project the standard spin coating method with the positive photoresist by means of EVG 120 Coater/developer (shown in Figure 3.3) machine was used. In spin coating an excess amount of the photoresist will be placed on the wafer and the chuck would rotate with the very high speed to spread the photoresist equally all over the wafer with centrifugal force. The procedure is composed of a treatment with HMDS vapour with

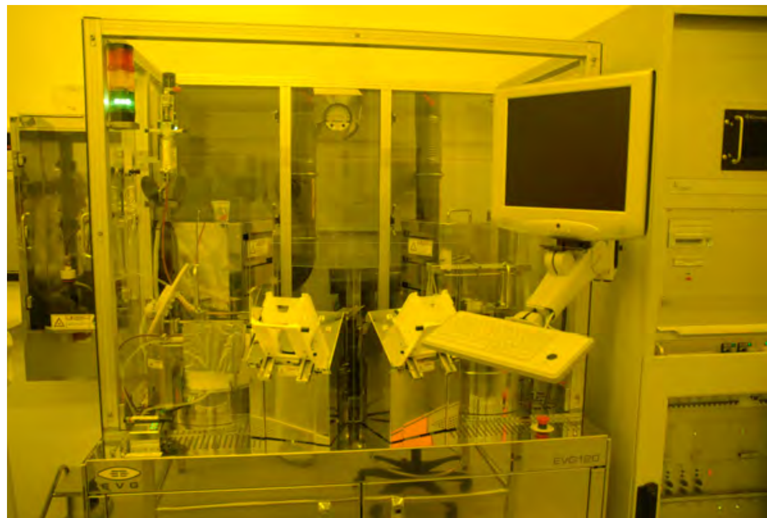


Figure 3.3: EVG 120 coater/developer

nitrogen as a carrier gas, spin coating with Shipley *SPR*3012 positive photoresist, and a soft bake at 95° C for 1 minutes. The temperature of the hotplate and the related humidity ($48 \pm 2\%$) in the room should be controlled. The coating Co-zero layer will be done by choosing the recipe on the computer. The resist thickness is $1.4\mu m$ and The recipe is 1-co-3012-zero layer. The recipe with option of no EBR should be selected. EBR is referred to edge bead removal, which clean the edge of the wafer from the photoresist. This will resolve the non uniformity of the photoresist on the edge of the wafer.

3.2.2 ALIGNMENT AND EXPOSURE

All the processes usually starts with the zero layer lithography. The alignment marks will be exposed on the zero layer coated photoresist and then etch into the wafer. In zero layer lithography the alignment markers would be etched into wafer substrate before the any further procedure. In the further processing all the mask would be aligned into these zero level marks. The zero layer alignment further will be used for aligning the different masks to the wafer for multi-layer patterning. In the following figure an example of alignment markers are shown.

Figure 3.4: Zero alignment marks on the silicon wafer

The procedure will be done with the ASML PAS 5500/80 automatic wafer stepper. The following mask, recipe and energy were used: COMURK mask, litho job *epi*0.0 and exposure energy of $150 mJ/cm^2$.

3.2.3 DEVELOPMENT

Use the EVG 120 developer to develop the wafers, Follow the the manual for the operation instructions for this machine.Use the program: Dev - Single Puddle (DEV-SP). The procedure is composed of a post-exposure bake at 115oC for 1.5 minutes, followed by a development step using Shipley MF322 developer (single puddle process), and a hard bake at 100oC for 1.5 minute.

3.3 PLASMA ETCHING OF ALIGNMENT MARKS

Follow the the manual for the operation instructions for this machine (OMEGA). The procedure terms of this etch program should not be changed. Control and set the plate temperature to 20°C, use the recipe : urk_npd to etch 120*nm* into the silicon.

3.4 REMOVING THE PHOTORESIST

3.4.1 STEP1 : TEPLA

Plasma strip Use the Tepla plasma system to remove the photoresist in an oxygen plasma. Follow the instructions specified for the Tepla stripper, and use the quartz carrier. Use Program 1: detects end point plus 2min over etch.

3.4.2 STEP2 : HNO3 99%

Cleaning : Use wetbench "HNO3 (100%)" and the carrier with the red dot. 10 minutes in fuming nitric acid (Inside: HNO3 (100%), selectipur; ambient temperature).

Quick Dump Rinser : Rinse for 5 minutes in the Quick Dump Rinser with the standard program until the resistivity is $5M\Omega$.

3.4.3 STEP3 : HNO3 65.5%

Cleaning : For 10 minutes in concentrated nitric acid (Inside: HNO3 (65%), selectipur; temp. 110 ° C).

Quick Dump Rinser : Rinse for 5 minutes in the Quick Dump Rinser with the standard program until the resistivity is 5 $M\Omega$.

Drying : Use the Avenger "rinser/dryer" with the standard program, and the white carrier with a red dot.

3.5 DEPOSITION OF THE HARD MASK WITH PECVD

use the Novellus machine and follow the manual for the operating operating instructions. Grow 3um of oxide on both sides of wafer. Use $xxx_sto2std$ recipe. The time is needed for etch is predictable from the growth rate of prior users. usually 110 seconds for 3um thickness. control that if TEOS is on and all the switches are in the TEOS mode.

3.6 MEASUREMENT OF THE THICKNESS

For the hard mask layer thickness measurements the microscope and program 5 point-Novellous STD oxide on Si is used. This is also popular by program number '45'. Note to choose no calibration.And to control the average, standard deviation, min and max values use the state bottom. 3.1

Mean	3102.483
Standard deviation	3.353
Min	3099.13
Max	3107.48

Table 3.1: Mean and Standard deviation

3.7 PATTERNING

3.7.1 COATING

Work with the EVG 120 Coater machine to coat the wafers with photoresist,and follow the manual for the operating operating instructions. The procedure is composed of an operation with HMDS vapour with nitrogen as a carrier gas, spin coating with Shipley *SPR*3012 positive photoresist, and a soft bake at 95 °C. for 1.5 minutes. Always control the temperature of the hotplate (21°C - 23 °C) and the relative humidity ($48 \pm 2\%$) in the room first. Work with the coating recipie $Co-3027-3.1\mu m$ (No EBR) with resist thickness: $3.0\mu m$. Note: to use a recipie with no EBR otherwise in for the etching Vias step , the surrounding side of wafers would be so fragile and breaks in parts.

3.7.2 EXPOSURE THE PATTERN

Work with ASML PAS 5500/80 automatic wafer stepper.and follow the manual for the operating operating instructions. Use SEOUXo1-VI mask from BOX 413.

RETICLE ID: 3x3
Diameter : $6mm$

LAYER depends on the picture:

1. Wafers M1 & M2 $20\mu m$ - Image 2
2. Wafers M3 & M4 $50\mu m$ - Image 4
3. Wafers M5 & M6 $100\mu m$ - Image 8

And exposure energy $300mJ/cm^2$.
Select the job Diesize_$6nm$/DIE6x6_9IMG.

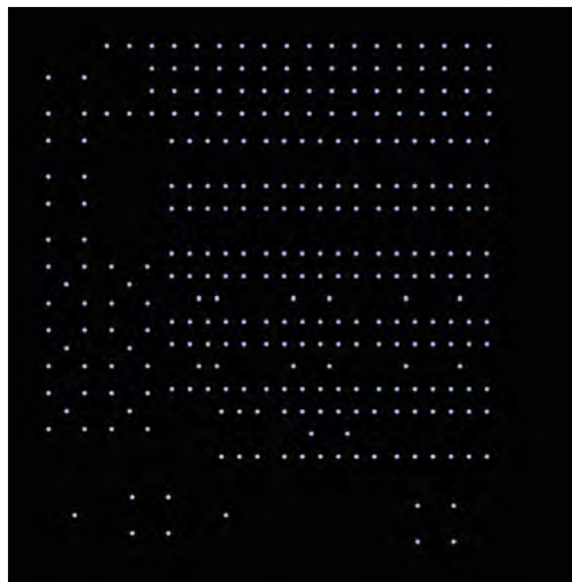


Figure 3.5: image4[**?**]

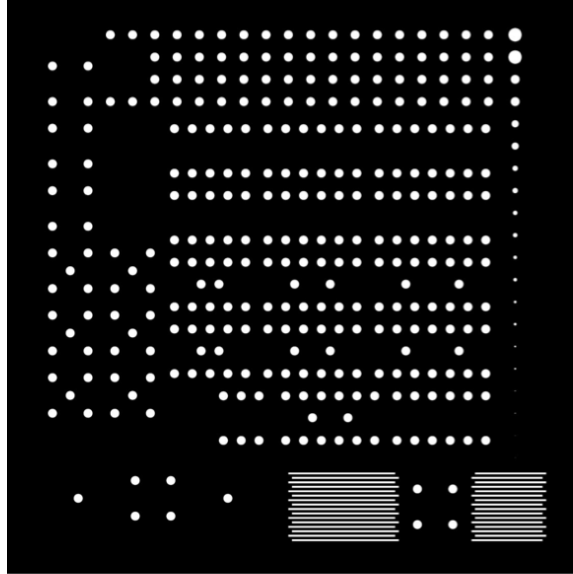


Figure 3.6: image8[?]

3.7.3 DEVELOP THE PATTERN

Work with recipe: DEV-SP.And choose six wafers and unload the wafer.

3.8 INSPECTION UNDER MICROSCOPE

Control the patterns with Inspect under MICROSCOPE.

3.9 ETCHING THE OXIDE IN PATTERNS

3.9.1 ETCH THE 3 μm HARD MASK WITH DRY TECH

Work with the Machine: DRYTEK and use the Program: STDOXIDE. It's not permitted to change the procedure conditions from the etch recipe and is only possible to change the etch maximum time, which depends on the patterns.
Assume that 10 minutes should be sufficient. The over etch is allowed and not cause problems.The aim is to remove all Si.

DRYTEK ***** DRYTEK****** I had some issues here , the vias were not etch totally initially

3.10 ETCHING THE SILICON THROUGH VIAs

Work with the Rapier Machine and To open the door and load cassette use VCH. Cassette module - Wafer module - Clean Cassette recipe is:Waferview. Module or etch recipe is : Straight trenchxxxC - 10DegClean. Only Change the cycles. The cycles can be changed in editor's icon from the square (2nd) placed on the right side

of the main screen column E2. Number of loops and Usually:
650 cycles for a depth of 300μm for 100μm thickness Diameter.
700 cycles for a depth of 300μm for 50μm thickness Diameter.
800 cycles for a depth of 300μm for 20μm thickness Diameter.
Click the hand symbol to load this. And Click on the wafer symbol on the bottom left to see if it has loaded.

rapier **** I did first time test with 6 wafer , two 100 micrometer diameter , two 50 micrometer diameter,another two 20 micrometer diameter. first time , i could have etch through only 100 micro meters diameter with 650 cycles. but some of my wafer are broken because at the step of zero layer coating i didn't use the recipe with no EBR. Second time processing i choose 90 wafer , each diameter 3 wafer*****

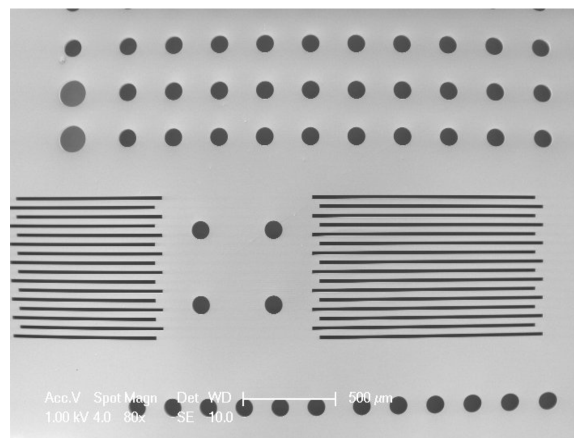


Figure 3.7: image8[**?**]

3.11 REMOVE THE PHOTORESIST

Tepla
Stripping resist: Use the Tepla Plasma 300 system to remove the photoresist in an oxygen plasma. Follow the manual for the operating instructions for the Tepla stripper, and use the quartz carrier. Use program 4: 1000 watts power for 15 minutes. Repeat this program to bring the total etch time to 30 minutes.

3.12 REMOVING THE OXIDE

BHF
Etch: Use wet bench "BHF 1:7 (SiO2-ets)" at ambient temperature, and the carrier with the blue dot.
The bath include a buffered HF solution.
Time: Etch until the backside of the wafers is hydrophobic(no water drop on it), add an extra 30 seconds.
The appropriate etch time depends on the layer thickness and composition.
The etch rate of thermally grown oxide is $1.3 \pm 0.2 nm$/s at 20°C.
Rinse: Rinse in the Quick Dump Rinser with the standard program until the resistivity

Table 3.2: Silicon nitride deposition conditions for the recipe

Process conditions from recipe 4INCHST			
Gasses & flows	Pressure	Temperature	Time
$SiH_2Cl_2/NH_3 = 169.5/30.5\ sccm$	150 $mTorr$	850^oC	**Variable command**

is $5M\Omega$. Dry: Use the single wafer dryer, note that wafers with through silicon vias are very fragile. Make sure the wafer is mounted correctly in the dryer and avoid stress on the wafer while loading and unloading. Inspection: Visually, through a microscope. All the windows must be open and the hydrophobic test may be applied.

3.13 REMOVING THE RESIST

3.13.1 STEP1 : TEPLA

Plasma strip Use the Tepla plasma system to remove the photoresist in an oxygen plasma. Follow the instructions specified for the Tepla stripper, and use the quartz carrier. Use Program 1: detects end point plus 2min over etch.

3.13.2 STEP2 : HNO3 99%

Cleaning : Use wetbench "HNO3 (100%)" and the carrier with the red dot. 10 minutes in fuming nitric acid (Inside: HNO3 (100%), selectipur; ambient temperature).

Quick Dump Rinser : Rinse for 5 minutes in the Quick Dump Rinser with the standard program until the resistivity is $5M\Omega$.

3.13.3 STEP3 : HNO3 65.5%

Cleaning : For 10 minutes in concentrated nitric acid (Inside: HNO3 (65%), selectipur; temp. 110 ° C).

Quick Dump Rinser : Rinse for 5 minutes in the Quick Dump Rinser with the standard program until the resistivity is 5 $M\Omega$.

Drying : Use the Avenger "rinser/dryer" with the standard program, and the white carrier with a red dot.

3.14 SILICON NITRIDE DEPOSITION

LPCVD furnance
The deposited thickness depends on the deposition time which can be calculated from the average deposition rates during recent furnace usage. An extra test wafer can be deposited to measure the thickness of the deposited layer.

3.15 MEASURING THE THICKNESS OF THE SILICON NITRIDE

MPV-SP

Leitz MPV-SP measurement system was used to measure the layer thickness. The instruction manual was followed for the measurement procedure.

3.16 cleaning

3.17 sputtering the Cu front side

PVD

3.18 sputtering the CU back side

3.19 Spray coating front side

when the topography on the surface of the wafer is high, The spray coating is used. This technique allows to less resist consumption and can coat arbitary shaped and textured substrates.The photoresist is spray on all over the wafer but the result is not homogeneous.

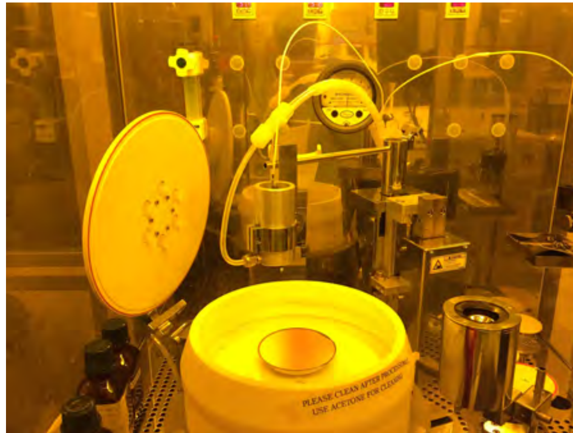


Figure 3.8: image9[**?**]

TheThe recipe *high pressure_2ml_1000mbar_6xlayer* was used for the spray coating. In the next step the wafer should be baked on a hotplate with the temperature of $115^{o}C$ for 3 minutes.

3.20 Pattering the front side

3.20.1 Contact aligner

EVG420 manual contact aligner in the class100 litho-room was used in this step.

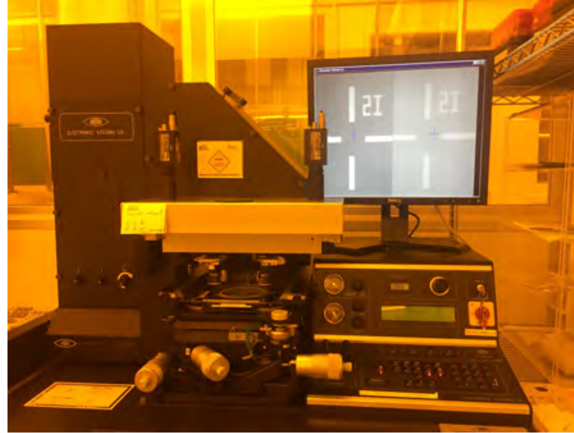


Figure 3.9: EVG420 contact aligner

First we have to align the wafer to the mask. There are a set of dark and transparent sheets in the cleanroom that can be used for finding the right alignment mark. By comparing the alignment marks on the mask and wafer (zero layer) a specific alignment mark (2I mark in this case) is chosen to align the mask and wafer.

To define the exposure time we used the following equation:

$$\text{exposure time } [s] = \frac{\text{exposure dose } [mJ/cm^2]}{\text{intensity } [mWatt/cm^2]}$$

Based on the provided table in the cleanroom for different types and thicknesses of resists the required exposure dose for this resist is $495/[mJ/cm^2]$.

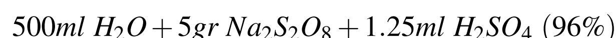
$$\text{exposure time}[s] = \frac{495}{17.6} \approx 28.125[S]$$

3.20.2 Development

The dedicated glassware for the copper was used for the developing the resist layer. First the $1/3$ *AZ400K* developer was diluted with $2/3$ of *Deionized (DI) water*. The wafer was developed for 1 minute in the aforementioned solution and rinsed for 3 minutes in DI water. In this step the pattern should be inspected on the wafer.

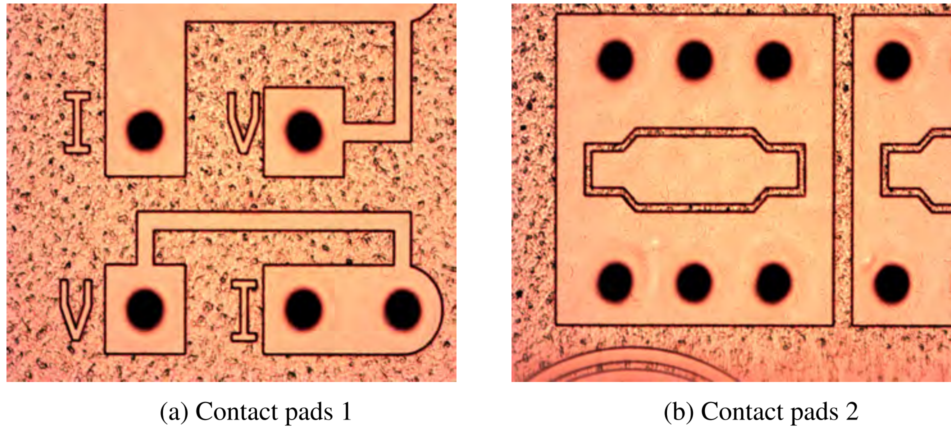
3.21 Etching the copper

Etch Cu layer with:



$$500ml\ H_2O + 5gr\ Na_2S_2O_8 + 1.25ml\ H_2SO_4\ (96\%)$$

Etch time approx 5 min. Visual inspect to see if this is too much or too little Rinse in DI water 5min. Dry using single wafer dryer. Inspection under the microscope: TiN is bluish.



(a) Contact pads 1 (b) Contact pads 2

Figure 3.10: Caption for this figure with two images

3.22 BACKING THE FILLED VTS WAFER

In this step the wafer after being filled by the nano-particle (nano silver\copper) is backed with the temperature of 250 degrees in a oxygen free furnace to void the oxidization of the copper.

Chapter 4

MEASUREMENTS

4.1 ELECTRICAL PROPRIETIES

4.1.1 RESISTIVITY

BULK RESISTIVITY

One of the intrinsic electrical proprieties which is relevant to carrier drift in materials like semiconductors and metals is The Bulk resistivity, shown by ρ. The definition of resistivity in solid state with the assumption of the homogeneous semiconductor material, explain the proportionality of the drift current density with the electrical field.

$$J = (1/\rho).E \tag{4.1}$$

And the microscopic description is:

$$\rho = \frac{1}{q(n\mu_n + p\mu_p)} \tag{4.2}$$

where q is the electronic charge n and p electron and hole concentration, and μ_n and μ_P are the electron and hole mobility. In n-type (donor doped N_D) or p-type (acceptor doped N_A) the dopants are dominant and the equation is reduced as follow:
for n type

$$\rho \approx \frac{1}{qn\mu_n} \tag{4.3}$$

for p type

$$\rho \approx \frac{1}{qp\mu_p} \tag{4.4}$$

for this equations is seen that the resistivity is relevant to the number of free carries and their capability to moving in the lattice. In a figure below is shown the geometrical dimensions of the bulk resistance.

In this figure the resistivity is:

$$\rho = \frac{RA}{L} \tag{4.5}$$

The unit of the measurement is Ωm or perferably Ωcm. Where R is the resistance of a square of side L. A is the cross sectional area, which is Wt. L is the distance

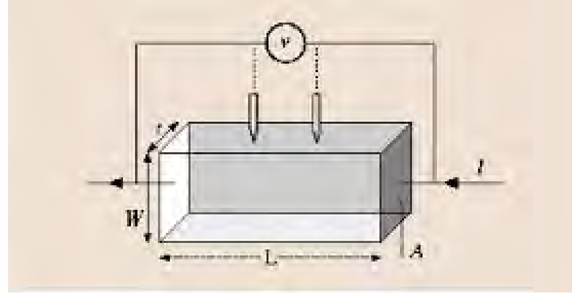


Figure 4.1: Geometrical dimensions of Bulk resistance[**?**]

between the two ideal contacts. Commonly sheet resistance (ρ_s) is more used, which bulk resistivity (ρ) divided by the thickness (t). R_{square}=ρ_S is the sheet resistance and mostly more used. [**?**]

CONTACT RESISTIVITY

4.2 MEASUREMENT OF THE RESISTANCE OF VIAs

Here for measuring the resistance for the VIAs The Kelvin structure is used.

4.2.1 CONTACT RESISTANCE

4.2.2 MEASUREMENT TECHNIQUES

KELVIN STRUCTURE

TRANSMISSION LINE MODEL STRUCTURE

4.3 XX

Chapter 5

Conclusions and Future Work

test

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Appendix A

Glossary

In this appendix we give an overview of frequently used terms and abbreviations.

foo: ...

bar: ...