Semiconductor Packaging University Program

For industry participants

CITC

Chip Integration
Technology Center

HAN_UNIVERSITY
OF APPLIED SCIENCES

Securing the future of the semiconductor industry in Europe

Together with HAN University of Applied Sciences, CITC developed the Semiconductor Packaging University Program. The program provides a connection between education and industry and as such contributes to the training and skills of people that align with industry needs. People who are in high demand – now and in the future. The program therefore represents an important step in securing the future of the semiconductor industry in Europe.

The program offers its participants training in all relevant aspects of chip packaging, both in theory and in practice. The theoretical part is provided by industry experts – in addition to CITC and HAN, the program was developed in collaboration with NXP, Nexperia, Ampleon, TU Delft and TNO. The practical assignments of the program are carried out on the premises of CITC and several semiconductor companies.

Why follow this program?

- Multidisciplinary
- Lectures by industry experts
- Hands-on approach
- Mix of company employees and students

CITC was founded in 2019 with strategic partners TNO and Delft University of Technology and is supported by local and regional governments. Based on Novio Tech Campus Nijmegen, CITC is perfectly situated in the heart of the Dutch semiconductor industry.

About CITC

Without advanced packaged and integrated chips, we can't live in smart houses, drive autonomous cars or communicate through 5G networks. Future societal challenges in energy, healthcare, mobility, agriculture and food mean that an increasing degree of intelligence must be built into products and services. As a key enabling technology, chips and their packages make this intelligence possible.

Solutions to societal challenges

Chip Integration Technology Center (CITC) is a non-profit, joint innovation center specializing in heterogeneous integration and advanced chip technology. We bring leading innovations in chip integration and packaging technology to market in a selected and growing number of application areas. In this way, we provide solutions to societal challenges: integration for tomorrow.

CITC has created an effective ecosystem in which companies, research and educational institutes work on bridging the gap between academics and industry. Together, we work on a new generation of packages providing smart, safe and rugged housing for chips. CITC's contribution to the ecosystem is to provide access to innovation, infrastructure and education.

Access to innovation

CITC runs its research programs in close collaboration with partners and customers. Our research efforts are focused on four program lines:

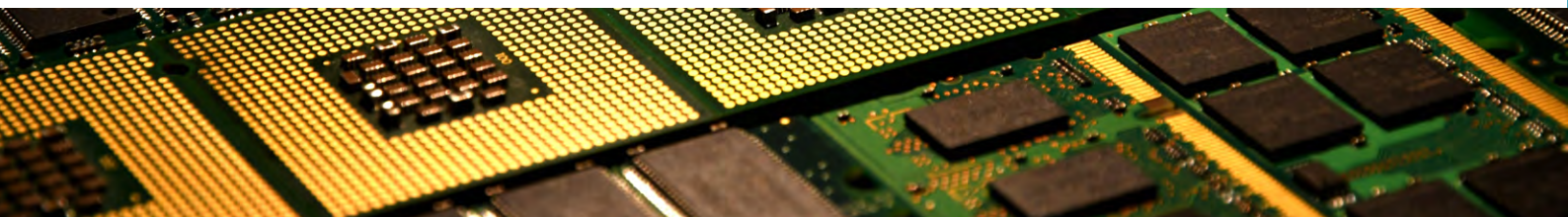
- Thermal High-Performance Packaging
- RF Chip Packaging
- Additive Packaging Manufacturing
- Integrated Photonics Packaging

Access to infrastructure

CITC's lab facilities support the innovation and education programs. Our lab also serves as a demo and application lab for new types of equipment and materials. It is available to third parties to enable them to develop, test and implement new packaging solutions.

Access to education

Education and training are key to securing the future of the semiconductor industry in Europe. In close cooperation with companies and educational institutes, CITC organizes targeted education and training for young talent.



Practical details

The Semiconductor Packaging University Program is accessible to professionals working or interested in the semiconductor industry, who are keen to expand or deepen their knowledge of semiconductor assembly and packaging. If you want to participate in the program but are not working in the semiconductor industry, an admission interview is required.

For industry participants, the program offers two options:

Theoretical part only

Location:	both online and onsite at Novio Tech Campus, Transistorweg 5T, Nijmegen, the Netherlands
Language:	English
Duration:	7 weeks, assessment is optional
Study load:	± 20-24 hours per week - lectures + self-study
Costs:	€ 2,750 excl. 21% VAT* + study material (approximately € 200)
Start date:	first week of new academic year - end of August/beginning of September

Both theoretical and practical part

Location:	onsite only at Novio Tech Campus, Transistorweg 5T, Nijmegen, the Netherlands
Language:	English
Duration:	**theoretical part:** 7 weeks, assessment is optional **practical part:** one full working week
Study load:	± 20-24 hours per week - lectures + self-study
Costs:	€ 3,750 excl. 21% VAT* + study material (approximately € 200)
Start date:	first week of new academic year - end of August/beginning of September

Both options require a bachelor's level of work and thinking.

Are you interested in joining this course?
Please contact us at **info@citc.org** to receive the registration form.

**VAT is not applicable for private participants*

"During the program, I attended lectures by people working at semiconductor companies such as NXP, Sencio, Enzyre and Nexperia. They covered the entire semiconductor industry from the 1980s-2020s. It's probably still the tip of the iceberg, but I've learned so much about the backend industry".

Mudit Goyal,
participant edition
2021-2022

Program description

Participants in the Semiconductor Packaging University Program learn about the semiconductor industry and take a deep dive into the final step of chip manufacturing. This is the phase in which the chip is packaged in its housing. Chip packaging is becoming increasingly complex and multidisciplinary, while costs must remain low. Developments such as integrated photonics, system-on-chip, embedded cameras, 5G antennas, sensors and micro-electro-mechanical systems place high demands on the manufacturing process... and the competences of semiconductor staff.

Setup
The program focuses on the design and manufacturing of semiconductor packages and the associated assembly, reliability and test techniques. It consists of two parts: a theoretical part and a practical part, the latter of which is optional. In the first part, you study the theory of semiconductor packaging and assembly:

- Semiconductor packaging
- Advanced applications
- Photonic assemblies
- Basic simulation and testing
- Quality and reliability

The duration of the theoretical part is one day a week over a period of seven consecutive weeks. You'll find more details on the next page under 'Program content'.

The second part consists of a one-week practical assignment in which you tackle a challenging semiconductor packaging problem. Please note, however, that the number of participants in this part is limited.

If your location does not allow you to attend the practical part in the Netherlands because of the distance, it is also possible to only follow the theoretical part.

> **"In my work, I have to deal with errors in the packaging of chips. This program helped me to better understand the processing steps of chip packaging. This way I can already identify where things went wrong in the process. That is very useful to us."**
>
> Gwen Visser,
> participant edition
> 2020-2021

Program content

Theme 1
Introduction to semiconductors and packaging

1A Front-end
- 1A.1 Microelectronics introduction
- 1A.2 Semiconductor physics overview
- 1A.3 Basic process technology steps (litho, etch, doping, ...)
- 1A.4 Integrated photonics introduction

1B Back-end
- 1B.1 Basic assembly and packaging steps (grinding, dicing, ...)
- 1B.2 Package families overview
- 1B.3 Die attach technologies
- 1B.4 Interconnect technologies
- 1B.5 Encapsulation technologies
- 1B.6 Application specific packaging-1 (RF, power, automotive, health)
- 1B.7 Application specific packaging-2 (MEMS and sensors)

Theme 2
Advanced applications

2A Application areas and associated requirements
- 2A.1 Consumer (mobile, multimedia, IoT, ...)
- 2A.2 Industrial and B2B (passports, credit cards, machines, ...)
- 2A.3 Aerospace and defense
- 2A.4 Health and medical (sensors, lab-on-chip)
- 2A.5 Automotive (engine control, autonomous driving, V2X, ...)

2B Advanced packaging techniques
- 2B.1 Water level packaging (WLP) principles
- 2B.2 WLP for ICs (WLCSP, FOWLP, FOMP, ...)
- 2B.3 WLP for MEMS (hermetic sealing, openings, ...)
- 2B.4 3D integration technologies
- 2B.4a Embedded die
- 2B.4b Interposer technologies
- 2B.4c Through package vias (TPV)
- 2B.4d Through silicon vias (TSV)
- 2B.4e Micro bumps
- 2B.5 Photonic assembly packaging
- 2B.6 Fundamentals of heat dissipation in 3D packages

Theme 3
Simulation and testing

3A Simulation
- 3A.1 Numerical methods in scientific computing
- 3A.2 Thermal simulations
- 3A.3 Mechanical simulations
- 3A.4 Design optimization

3B Testing
- 3B.1 Principles of testing
- 3B.2 Back-end test flow (wafer test, acceptance test, final test, ...)
- 3B.2 Tester functionality overview (architecture, probe cards, ...)
- 3B.4 Measurement accuracy (noise, calibration, sensing method, ...)
- 3B.5 Binning/sorting
- 3B.6 Data analysis and water maps
- 3B.7 Test jobs (architecture, limits, ...) and standards (JEDEC)

Theme 4
Quality, reliability and smart manufacturing

4A Quality
- 4A.1 Basic quality control concepts
- 4A.2 On-line and off-line measurements and tests
- 4A.3 Quality program techniques such as QFD, DoE and SPC
- 4A.4 Quality standards

4B Reliability
- 4B.1 Basic reliability definition, lifetime distribution and prediction methods
- 4B.2 Physical failure mechanisms in electronic components
- 4B.3 Package-related failures
- 4B.4 Reliability screening and testing
- 4B.5 Failure analysis methods
- 4B.6 Design considerations and system reliability
- 4B.7 Thermal management in relation to package reliability
- 4B.8 Case studies of different package types (low/high power, ...)

4C Smart manufacturing
- 4C.1 Challenges in manufacturing
- 4C.2 IT infrastructure requirements
- 4C.3 Examples: SNAP, BIM line, digital twin, scheduling

Contact

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