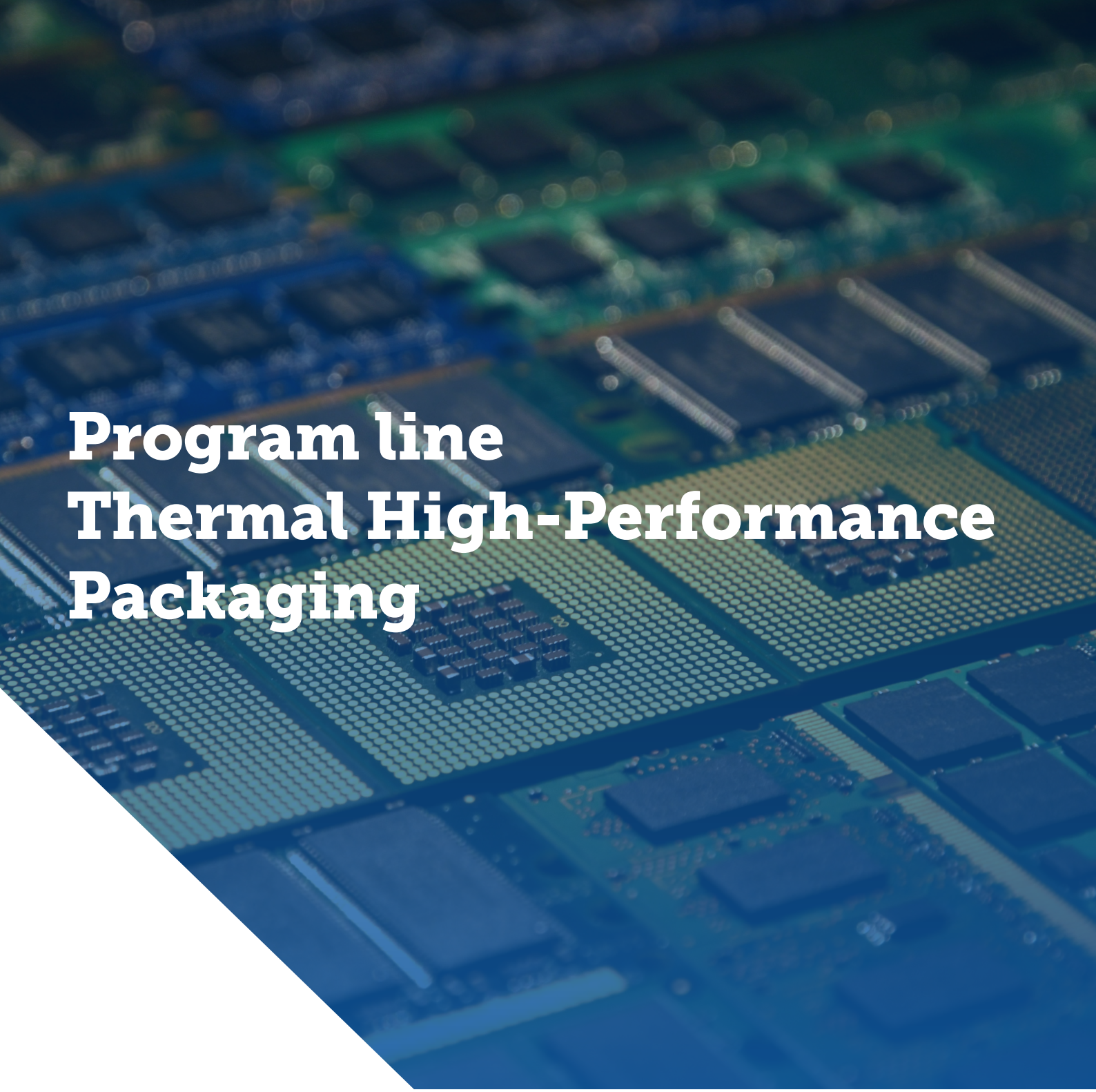


Program line Thermal High-Performance Packaging

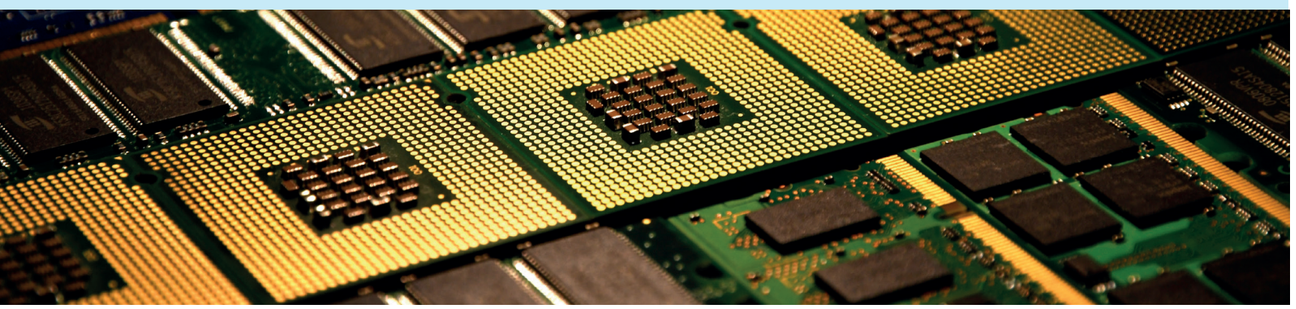
CITC

Chip Integration
Technology Center

The current energy transition is driving innovation towards more efficient and compact power electronics. Further miniaturization results in higher power density. This requires the development of new wide-bandgap semiconductors and improvements in thermal dissipation of the packages. Thermal dissipation is achieved through a die attach material bonding the semiconductor die to a heat transfer element. A critical challenge in this area is to improve thermal dissipation while retaining a high level of reliability.

CITC approach

Improving the thermal dissipation of semiconductor packaging is the main focus of CITC's Thermal High-Performance Packaging Program. Our approach to achieving this is through close collaboration between material suppliers, end users and equipment manufacturers. We conceptualize, model, and characterize novel thermomechanical design strategies and materials implemented in functional packages. The molded packages are composed of low-stress, highly reliable die attach solutions with high-power dissipation properties. We focus on generic solutions for pressure-less sintering on copper substrates that retain their advantages in price, processing, thermal and electrical conductivity.



CITC key competences

To identify, manufacture and validate packaging solutions, we rely on four key competencies:

1 Assembly and integration

In our labs, we have an advanced classical packaging infrastructure capable of manufacturing functional packages at an industrial quality level. The infrastructure is versatile to enable us to handle all levels of packaging.

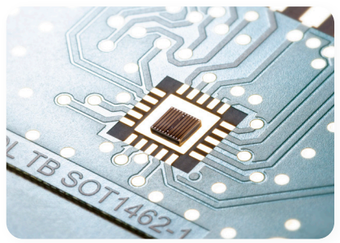
Our assembly capabilities:

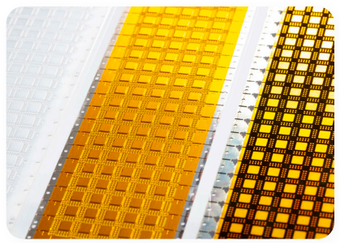
- Surface (plasma) cleaning/sample preparation
- Dispensing/glue-solder depositing, stencil printing
- Die bonding – glue-solder-sinter, pressure and pressure-less
- Wire bonding – wedge-wedge, ball/wedge, copper, aluminum
- Film-assisted transfer molding
- Wafer and package dicing

In addition to classical packaging, we have panel level package capabilities which we are actively developing to realize breakthrough technologies for Panel Level Power Packaging.

2 Thermomechanical modeling and simulations

We have extensive experience in thermal-mechanical simulation of semiconductor packages. Transient, viscoelastic and viscoplastic simulations provide valuable insight into the potential failure modes. Through theoretical insight, we can rapidly steer concept optimization and iterate towards a more reliable product. This makes it possible to shorten reliability tests, which traditionally take thousands of hours. The simulations support our understanding of failure by visualizing the stress distributions at play within the package.





3 Characterization and reliability assessment

We use functional packages to verify reliability based on the industrial AEC-Q100/101 standard. One of our standard test methods is thermomechanical cycle lifetime, where packages are repeatedly exposed to cold and hot environments. During cycling, the device properties are characterized to identify failure. Electrical, thermal (Zth/Rth), acoustic, X-ray and cross-section characterization are performed. This allows us to track potential failure modes through manufacturing and reliability testing processes.

Our characterization capabilities:

- Optical: laser confocal, microscopy
- Confocal scanning acoustic microscopy
- SEM/EDX, X-ray and cross sectioning
- Electrical MOSFET: RdsON, Rth/Zth

Our reliability analysis capabilities:

- Thermo-mechanical cycle lifetime
- Humidity/temperature testing

4 Advanced characterization

- In-situ reliability monitoring: in collaboration with Delft University of Technology (TUD) we have developed an in-situ reliability system that monitors package performance during thermal cycling. The setup allows us to assess changes in thermal performance as a function of temperature. The system can be applied to custom-made thermal test chips and to MOSFETs.

- Advanced die attach fracture characterization: in collaboration with Eindhoven University of Technology (TU/e), we are investigating the nature of the fracture modes in die attach materials. The insights obtained are used to improve our simulation models and to better understand the observed failure modes.

Chip Integration Technology Center

CITC is a non-profit, **joint innovation** center specializing in heterogeneous integration and advanced chip packaging technology. We have created an **effective ecosystem** in which companies, research and educational institutes work on **bridging the gap** between academics and industry. CITC was founded in 2019 with strategic partners TNO and Delft University of Technology and is supported by local and regional governments. Based on Noviotech Campus Nijmegen, CITC is **perfectly situated** in the heart of the Dutch semiconductor industry.

Contact

Chip Integration Technology Center
Transistorweg 5T
6534 AT Nijmegen, the Netherlands

+31 85 48 35 600
info@citc.org
www.citc.org

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