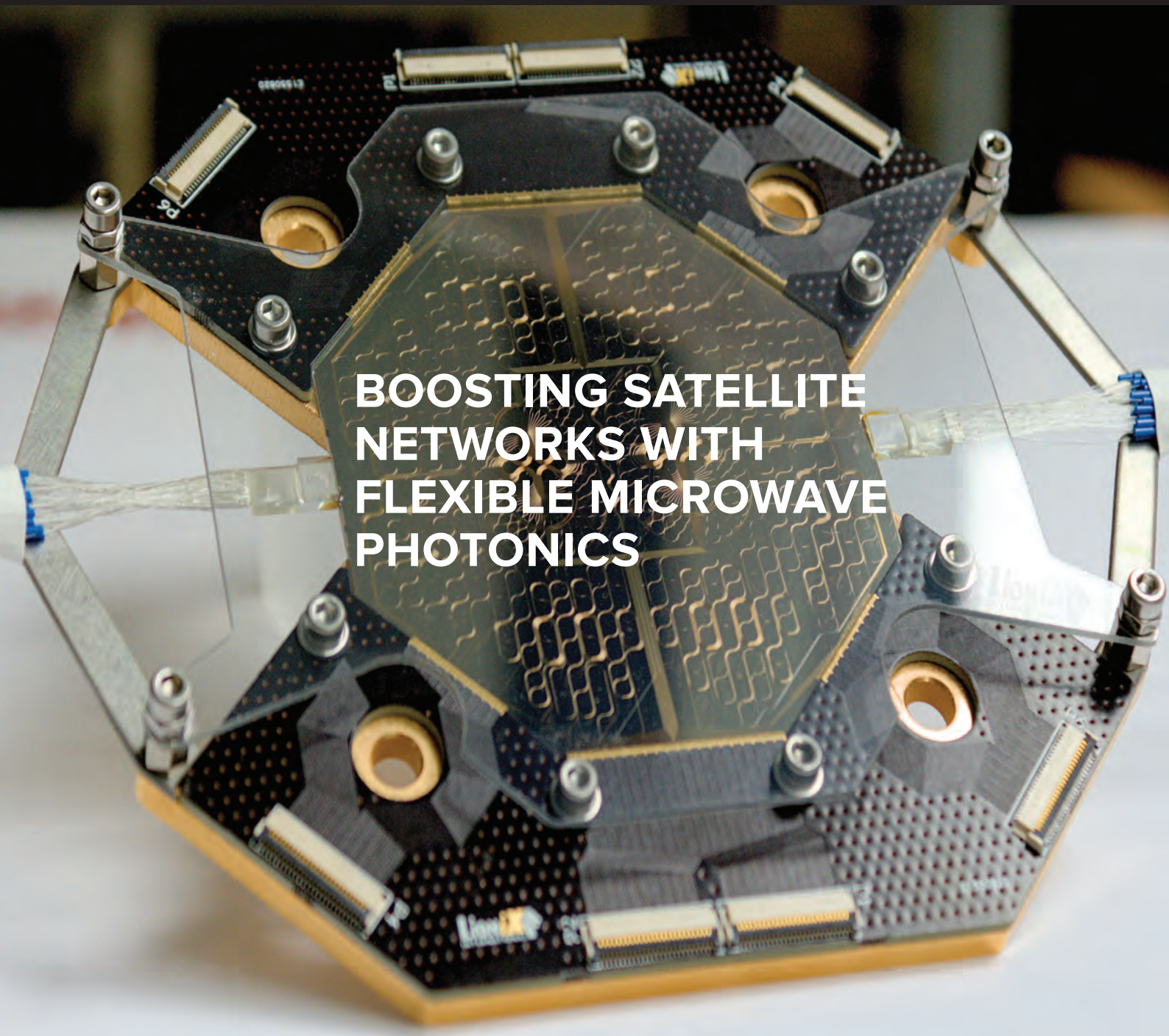




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BOOSTING SATELLITE NETWORKS WITH FLEXIBLE MICROWAVE PHOTONICS

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Advancing the semiconductorisation of chip packaging

The integrated photonics industry
needs scalable, cost-efficient
packaging processes suitable for
high volumes



Advancing the semiconductorisation of photonic chip packaging

The PIC industry needs scalable, cost-efficient packaging processes suitable for high volumes, like those in traditional semiconductor manufacturing. The Chip Integration Technology Center (CITC) and vario-optics are working on multiple projects to this end, including co-packaging EICs and PICs on a glass substrate, and evanescent coupling into polymer waveguides.

**BY NIKOLAUS FLÖRY & VALENTIN STRÄSSLE, VARIO-OPTICS,
SANDER DORRESTEIN, CITC, AND TAYNARA DE OLIVEIRA, TNO DELFT**

OVER THE LAST DECADE, PICs and related technologies have matured tremendously and found use in a multitude of devices. Silicon photonics platforms, for example, have expanded their range of applications beyond transceivers to photonic computing, biomedical sensing, optical interconnects, and consumer applications.

The recent push towards adopting optical solutions in AI/ML hardware has further spurred the development of multi-chip modules that require

high-density electrical and optical interconnects. These upcoming generations of PIC designs present common challenges in electrical and optical assembly and packaging, namely: increasing density (more functions per unit area); increasing bandwidth and reaching higher data rates while maintaining signal integrity; and developing cost-effective assembly processes for high-volume manufacturing.

So far, state-of-the-art assembly technologies developed for foundry-produced PICs have focused

primarily on supporting businesses with prototyping, low-volume manufacturing, and fibre pig-tailing (Figure 1). This has resulted in a poor level of standardisation and highly complex systems and processes that are only suitable for low volumes, making it challenging for new companies to adopt these methods and establish a viable business model in the market.

Another factor contributing to this landscape is that PIC products need to be considerably differentiated, both to achieve their technological aims and to stand out commercially. However, this leads to high assembly costs, especially compared to those in the established semiconductor industry; assembly makes up about 80 percent of the total costs of an integrated photonic device, compared with just 20 percent for typical semiconductor devices. To provide cost-effective photonics products – and thus keep up with increasing demands in the future – assembly methods must be simplified and made scalable. Addressing these cost challenges is essential for PICs to transition from niche solutions to mainstream applications, especially in consumer electronics, telecommunications, and biomedical devices, where affordability and scalability are critical.

Fortunately, the semiconductor industry offers a range of assembly and packaging processes with proven scalability and cost efficiency, presenting valuable insights and methods that can be adapted for PIC packaging. However, integrated photonics has unique requirements, so these processes must be tailored to meet the specific needs of high-density optical interconnects. This adaptation process, termed the “semiconductorisation” of PIC packaging, focuses on simplifying assembly steps while enhancing accuracy and scalability.

For instance, streamlined assembly techniques, like automated passive alignment, can significantly reduce per-unit costs. Recent pilot projects show that simplified panel-level packaging can achieve cost reductions of up to 30-40 percent compared to traditional fibre pig-tailing and discrete component assembly. Such benchmarks offer a promising roadmap for further cost-cutting strategies as PIC technology scales to higher production volumes, potentially making photonic solutions more accessible for a range of applications.

Scalable co-packaging of chipllets

Supported by the Dutch Growth Fund PhotonDelta, the Chip Integration Technology Center (CITC) is developing a scalable panel-level assembly concept addressing many challenges of integrated photonics packaging. CITC is collaborating on this project with vario-optics, which provides the key optical interconnect technology. The concept utilises advanced assembly technologies from the semiconductor industry, but is tailored to co-package EICs and PICs in a single package. In other words, this programme adds the “optical element” of advanced assembly at the panel level.

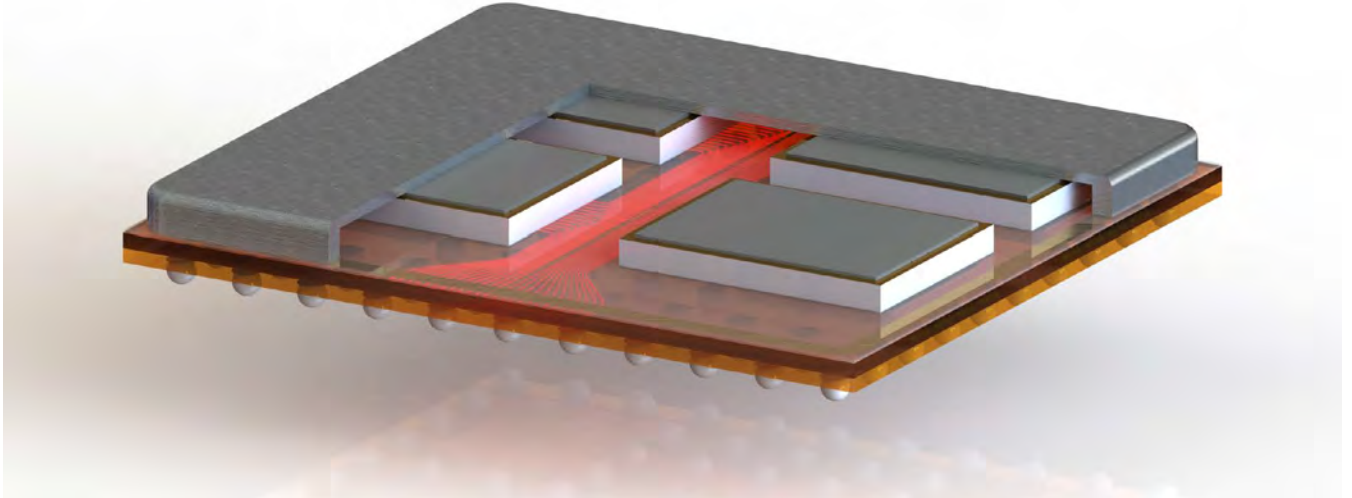
This concept, shown in Figure 2, is based on a panel-level fan-out design, where electrical and optical chipllets are mounted on the panel. Electrical and optical redistribution layers (eRDLs and oRDLs) enable chip-to-chip and chip-to-world communications in both domains. An oRDL is produced on one side of the panel and an eRDL on the opposite side. Using through glass vias (TGVs) the electrical interconnects cross from one side of the panel to the other. A flip-chip bonding process mounts both EICs and PICs on the panel.

Once the panel is populated, the assembly is covered by an overmoulding compound to protect sensitive components. Single modules are then created by cutting the panel in a conventional wafer dicing process. After this step, the module’s optical interface is accessible through a mechanical interface, which an optical connector can be plugged into, as shown in Figure 3. The end user can assemble the module according to the needs of their particular application, either in a land grid array or ball grid array.

Bearing in mind the key targets of scalability and cost-efficiency, every choice related to this packaging platform is made with the aim of simplifying the assembly process. This means



➤ Figure 1. Traditional way to optically couple to a PIC using direct attach fibre arrays units (FAUs). Such assemblies are suitable for companies seeking to assemble and package their (first) integrated photonic dies for prototyping. However, due to many discrete components involved, cumbersome footprints and loose fibres within the setup, such solutions are not suitable for mass-scale fabrication flows.



► Figure 2. Concept for advanced packaging for integrated photonics. On the top side of a glass substrate there is an optical redistribution layer, and on the bottom side an electrical one. Combined they enable chip-to-chip and chip-to-world communication.

using known semiconductor assembly processes, realising relaxed alignment tolerances at the panel scale or wafer scale, and enabling short process times.

Photonic interposer based on PCBs

Many of the features and benefits of optical interposers stem from the semiconductor and microelectronics industry. The key difference in applying this concept to photonics is the addition of an oRDL that is compatible with various substrates (PCB, glass, silicon) and can be connected to photonic chips. Planar waveguides based on polymer or glass are an excellent candidate to fulfil these requirements.

One of the biggest challenges in coupling light into PICs is their inherently small mode field diameter (MFD). PIC platforms with very high confinement, such as InP, can exhibit MFDs of the order of only 1 μm . Coupling standard SMF-28 glass fibres to such small MFDs results in high optical losses due to the mode field mismatch. Although spot-size converters are available on most PIC platforms today, they typically require additional steps in the manufacturing process and exhibit large footprints, both of which increase the costs per unit area on the wafer. Moreover, to connect them to glass fibres or fibre arrays, additional fan-outs are necessary.

Depending on the pitch size (127 μm or 250 μm) and number of I/Os, spot-size converters and fan-outs consume a comparatively large area of the wafer.

For economic reasons it therefore makes sense to relocate these features to another platform, and polymer waveguides can perform this

task. They can be manufactured in large quantities on different substrates such as glass or silicon wafers or PCB panels using UV lithography. Polymer waveguides also require far fewer process steps, decreasing the costs per area. Larger features like spot-size converters, fan-outs, splitters, and combiners can therefore be fabricated at minimal cost.

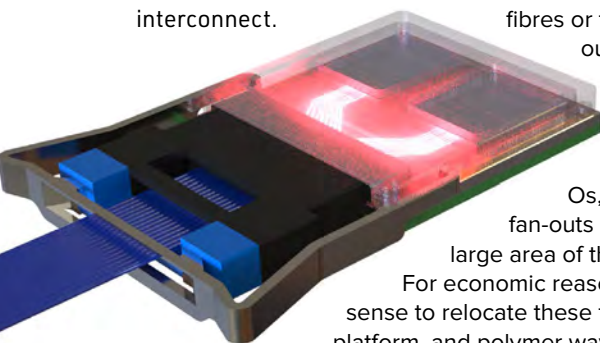
Furthermore, the dimensions of the cores and thus the MFDs of the polymer waveguides can be varied without any additional effort, even on the same chip (see Figure 4). Thus, different PIC technologies like silicon photonics, silicon nitride, and InP as well as glass fibres can easily be connected. All these capabilities make polymer waveguides a first-class technology platform for hybrid integration and photonics at the PCB and interposer level.

Standard PCBs can include features such as high-speed RF interfaces, (glass) interposers, thermal dissipation layers, and electrical vias. Depending on the application, the polymer waveguides can be fabricated on top of the PCBs or sandwiched into them to form the optical connections of the electro-optical board. The PCB can also be substituted with other carriers such as silicon wafers or glass sheets. As polymer waveguide technology has advanced, it now supports single-mode operation at most common wavelengths (O-, C-, 850-nm-band). Moreover, polymer waveguides show high power damage thresholds, good environmental stability, and compatibility with reflow soldering processes.

Low-loss coupling: the holy grail

There are several ways of optically connecting PICs to oRDLs: edge coupling, surface grating coupling, and surface coupling by adiabatic or evanescent field couplers. The most important factors in choosing a coupling technique are: alignment

► Figure 3. Optical module with pluggable fibre interconnect.





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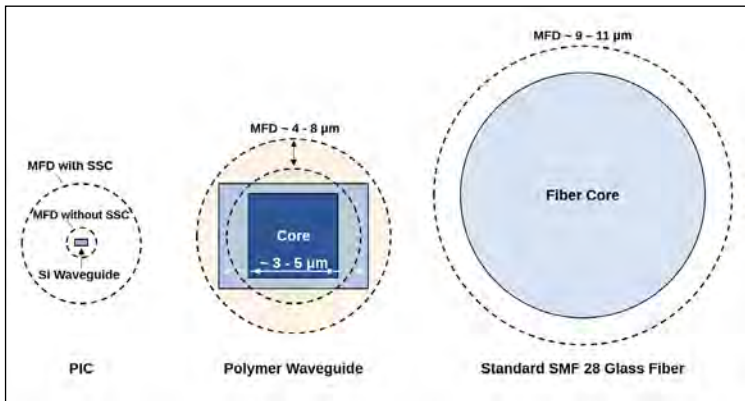
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OPTICA



► Figure 4. Planar polymer waveguide platform. Typical mode field diameters are: 1 μm for InP; 2 μm for silicon nitride; about 10 μm for SMF28 glass fibre; and adjustable between 4-8 μm for polymer waveguides.

accuracy requirements, optical losses, wavelength variation sensitivity, polarisation sensitivity, and testing possibilities. Figure 5 compares the advantages and disadvantages of different optical coupling schemes.

Edge coupling is a well-established scheme suitable for a variety of PIC technologies. Many concepts have been developed to overcome tricky alignment routines. In the H2020 project QAMeleon, for example, vario-optics developed a micro-machined silicon carrier to act as a substrate for both an active InP chip as well as a passive polymer fan-out circuit (see separate box). The 3D patterned carrier enables highly accurate passive alignment of the optical parts.

At the same time, recent improvements in assembly equipment and alignment routines have made active alignment more compatible even with high-volume manufacturing. CITC is investigating test vehicles in which a fibre assembly unit (FAU) with standard SMF-28 fibres is bonded to a polymer waveguide chip (Figure 6). The technique involves actively aligning the outermost fibres of the FAU to optical loops on the polymer chip. The two parts are bonded together when the signal of both loops is optimised. In a second step, the package is positioned and bonded to a silicon nitride PIC with similar alignment loops and small MFDs of 2 μm .

This configuration has demonstrated coupling losses on the order of only 1 dB per facet (polymer-to-PIC) – significantly better than direct fibre-to-PIC connections, which typically have coupling losses of close to 3 dB. Polymer waveguide interposers therefore meet the requirements for low-loss fibre-to-chip coupling or even chip-to-chip coupling.

However, there are limits to how much this technique can reduce the overall system losses, even with tailored polymer waveguide geometries. This is because there are geometrical limitations in optimising for two different interfaces within one waveguide, as well as limits to alignment accuracy. Using an alternative approach of evanescent field coupling offers a viable solution for circumventing these constraints.

Evanescent surface coupling

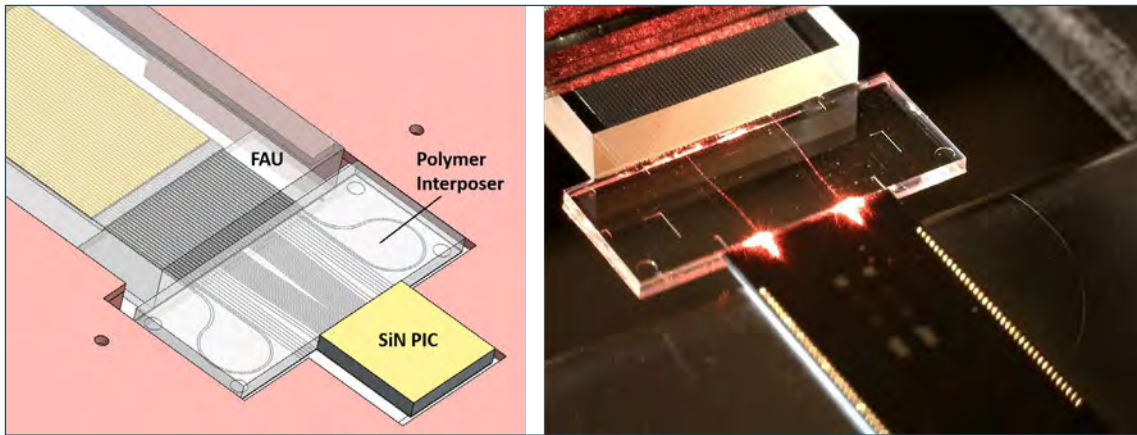
Evanescent coupling, commonly also referred to as adiabatic coupling, involves an energy transfer between overlapping evanescent fields in two waveguides. This technique relies on a near-field interaction at the surface interface, so it is essential to minimise the gap between the waveguide cores to increase the energy efficiency of the transfer. Both cores must therefore be exposed to allow for a low-loss coupling.

Figure 7 presents a schematic representation of the evanescent field coupling mechanism. In this process, light is out-coupled from the silicon nitride PIC via an inverted taper, which narrows to an optical tip, forcing the mode field out of the waveguide. During the assembly phase, this tapered section is aligned in proximity to the polymer waveguide on the oRDL, enabling efficient mode transfer whereby the light is captured and guided towards the package interface.

Results of design simulations highlight how optimising both the silicon and polymer waveguide structures can yield exceptionally low loss. For instance, using a 420 μm taper length with high refractive index contrast polymers results in coupling

► Figure 5. Comparison of different coupling schemes.

Edge Coupling	Grating couplers	Adiabatic coupling
<ul style="list-style-type: none"> ✓ Low Optical Loss ✓ Wavelength insensitive ✓ Polarization independent 	<ul style="list-style-type: none"> ✓ Place anywhere on the PIC ✓ Less critical alignment accuracy ✓ Wafer level test compatible 	<ul style="list-style-type: none"> ✓ Low loss solution ✓ Wavelength insensitive ✓ Wafer level test compatible ✓ Tolerant alignment
<ul style="list-style-type: none"> - Incompatible wafer level testing - High alignment accuracy required 	<ul style="list-style-type: none"> - Optical loss - Wavelength sensitive - Polarization dependent 	<ul style="list-style-type: none"> - BEOL constraint



➤ Figure 6. A concept for simultaneously interfacing a polymer interposer with both an FAU and a small-mode-field PIC silicon nitride PIC, involving active alignment.

losses as low as 0.2 dB at a wavelength of 1550 nm. Extending the taper length to 900 μm further reduces the coupling loss to just 0.08 dB, which is very promising compared to the state of the art.

Furthermore, redesigning not only the taper but also the overall chip – including adjustments to refractive index contrast, cladding materials, and other factors

– can minimise the footprint of these interconnects to hundreds of microns while maintaining coupling efficiency above 95 percent.

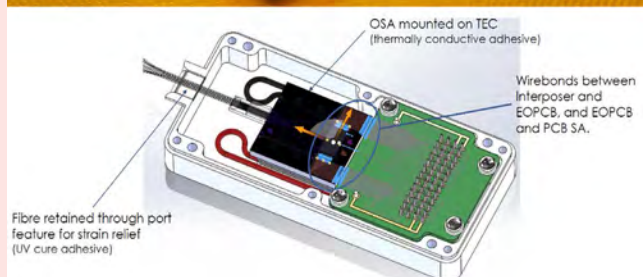
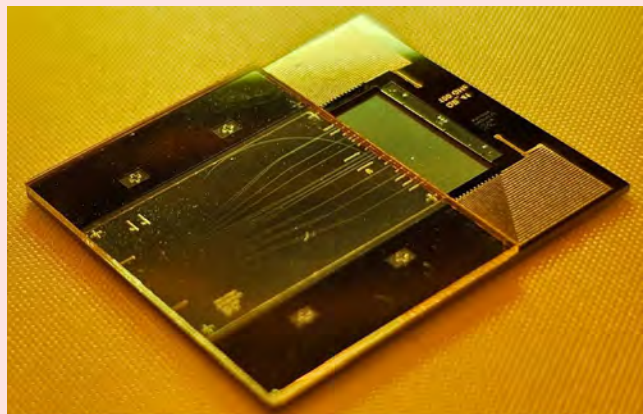
This approach also relaxes lateral alignment tolerances to approximately $\pm 2\ \mu\text{m}$ for both transverse electric (TE) and transverse magnetic (TM) polarisations. Previous experimental studies,

QAMeleon Project

THE H2020 QAMeleon project aimed to scale metro and core networks by providing faster, cheaper, and more compact optical components for generating, switching and receiving light under an automated, software-defined-networking (SDN) enabled environment. The different hardware developments are aimed at achieving ultra-high rates of up to 128 Gbaud and more than 3 Tb/s capacity on a single carrier, while reducing the energy consumption per bit.

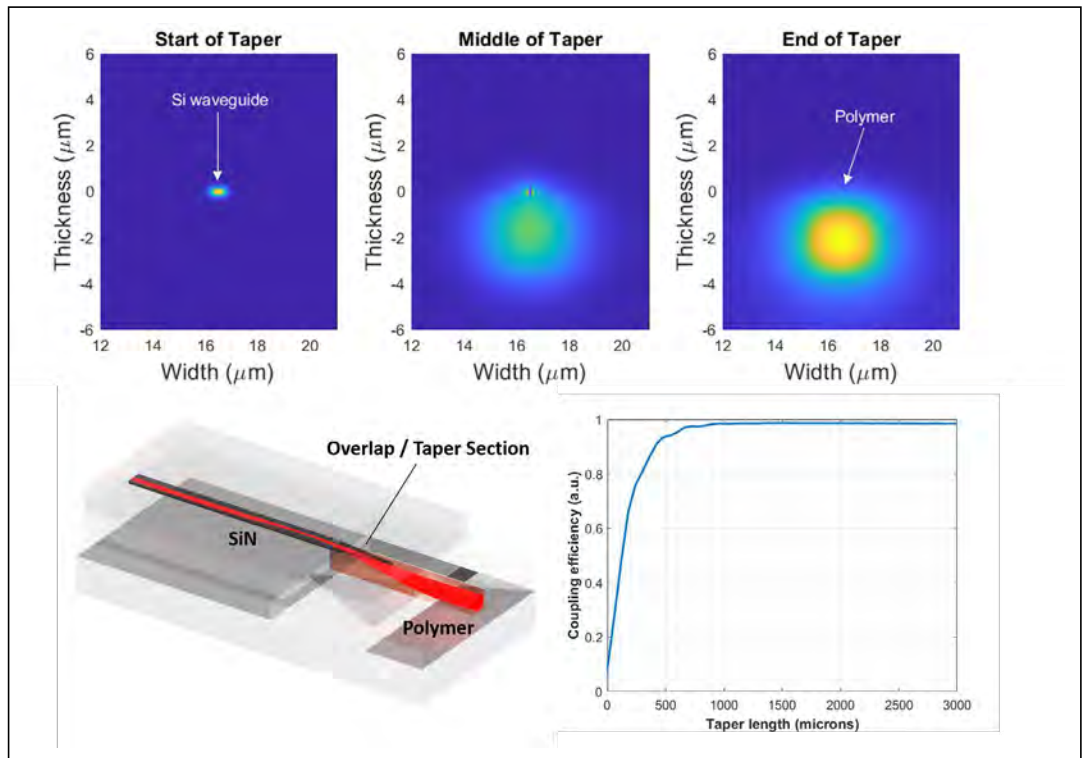
An essential part of this network is the InP-based wavelength selective switch, which can route different wavelengths from a single input into any one of N multi-wavelength outputs. The InP waveguides used, which exhibit a small mode field diameter of around 1 μm , are very challenging to connect directly to glass fibres, and would result in low density of optical I/Os limited by fibre cladding diameter. Therefore, InP chips were instead connected to an optical interposer, which can convert the mode field to match that of glass fibres. In addition, the optical I/Os were fanned out to make the best possible use of the space on the PIC.

The QAMeleon project developed a solution for a passive alignment between the PIC and optical interposer with <1 μm alignment accuracy, by placing the PIC and the polymer waveguide chip on a 3D patterned carrier. The carrier has different, very well-defined reference planes so the optical axes of the InP and polymer cores are aligned. Additional mechanical stops and alignment marks help to assemble the parts with an accuracy better than 1 μm .



Standard fibre arrays can be attached to the polymer optical interposer. The carrier is also equipped with electrical fan-out to connect the PIC electrically. This package consisting of PIC, waveguide chip, and electro-mechanical carrier form an electro-optical subassembly that can be easily connected to other components in a network.

► Figure 7. Results from optical simulations of an adiabatic coupling interface. The modelling allows the extraction of critical taper dimensions on silicon nitride. Coupling losses of ~0.08 dB (98 percent coupling efficiency) can be achieved for a taper length of 1000 μm at a wavelength of 1550 nm. This is much more efficient compared to the industry standard of 1 dB for regular edge-coupling interfaces.



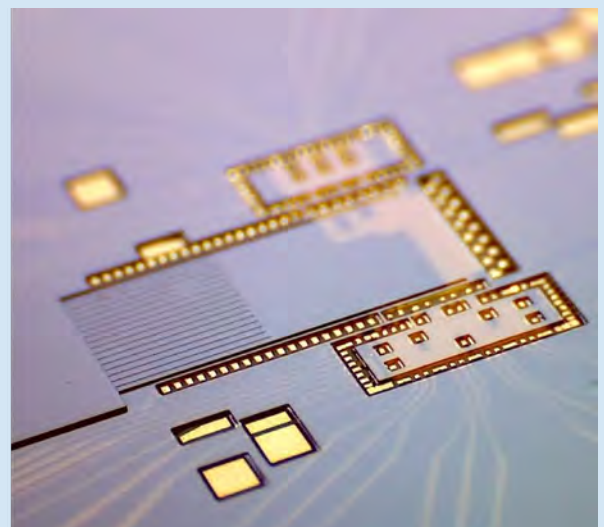
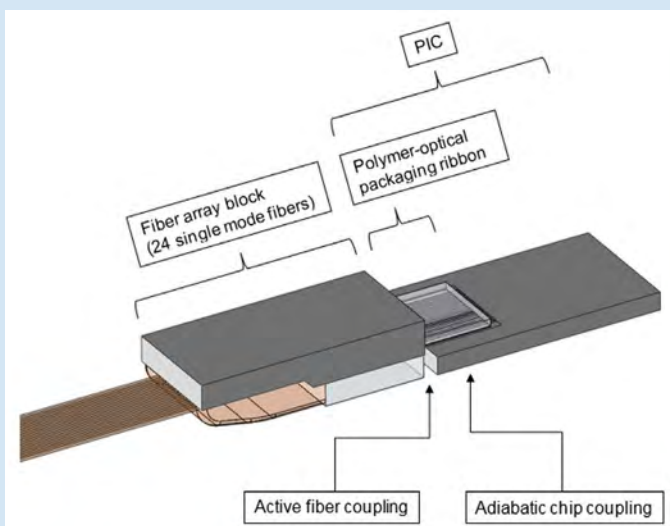
ICT-STREAMS Project

ADIABATIC COUPLING allows efficient light transfer from tapered silicon waveguides to the polymer waveguide platform. Prior works using FAU-attached polymer ribbons achieved fibre-to-polymer-to-PIC coupling losses of < 1.2 dB (left picture, demonstrated within ICT-COSMIC).

The H2020 ICT-STREAMS project focused on developing high-data-throughput communication between multiple computing nodes based on a silicon photonics platform using any-to-any optical connections. As part of the project, vario-optics developed a multi-socket optical PCB based on the polymer platform described in this article. The final

oPCB consisted of an RF electrical interface with small metal pads (125 μm pitch) and a (transparent) polymer layer featuring optical waveguides with exposed cores (right picture).

The device achieved low insertion losses over a wide spectral bandwidth, as well as relaxed alignment tolerances of $\pm 2 \mu\text{m}$. The broad operating wavelength range (> 100 nm) is particularly important for WDM applications. This system successfully demonstrated operation at a line rate of 50G per channel with an energy consumption of only 5 pJ/bit.



conducted independently by IBM and vario-optics, have already demonstrated the strong potential of this technique, achieving total coupling losses of less than 1.2 dB for a fibre-to-polymer-to-PIC setup, and showcasing the PCB-integration of adiabatic coupling interfaces, as demonstrated within the EU project ICT-STREAMS (see separate box).

While these results prove the viability of this scheme, previous realisations have been constrained by non-ideal planarity of PCB substrates and the limited availability of PICs with accessible core layers. In recent years, however, several foundries have added these features to their PDKs. Beyond that, the use of a glass substrate for both eRDLs and oRDLs is a great choice in terms of planarity for such an interface, finally allowing full exploitation of the advantages of evanescent coupling.

Outlook on scalable manufacturing for PIC packaging

Advanced and scalable panel-level processes, together with efficient coupling methods, hold great promise to fulfil the key requirements of future PIC packaging: low-loss optical interconnections with $\ll 1$ dB (20 percent) optical loss from PIC to oRDL; relaxed alignment tolerances $\gg 1 \mu\text{m}$; and cost-effective assembly methods of PIC to substrates with automated passive alignment.

FURTHER READING / REFERENCE

- **Integrated Photonics Roadmap by CITC:**
<https://www.citc.org/resources/uploads/2024/04/CITC-Integrated-Photonics-Technology-Roadmap.pdf>
- Electronic-photonic board as an integration platform for Tb/s multi-chip optical communication:
<https://doi.org/10.1049/ote2.12017>
- Highly reliable polymer waveguide platform for multi-port photonic chip-packaging:
<https://ieeexplore.ieee.org/document/9501540>

Both edge coupling and evanescent coupling schemes used in such a photonic interposer platform can provide excellent performance.

Each use-case requires a system-level evaluation to identify the most suitable coupling scheme, balancing efficiency, assembly tolerances, and most importantly cost per assembly.

In all cases, integrating both electronics and photonics in a single package is a key prerequisite for the successful semiconductorisation of PIC assembly and photonic packaging.



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